# CUET PG 2026 Computer Science Question Paper

| **Time Allowed :**3 Hours | **Maximum Marks :**300 | **Total questions :**75 |
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## General Instructions

**Read the following instructions very carefully and strictly follow them:**

1. The Question Paper consists of 75 Multiple Choice Questions (MCQs).
2. Total marks for the exam is 300.
3. The total duration is 90 minutes; a, timer on the screen will display the remaining time, and the exam will automatically submit when the time reaches zero.
4. For every correct answer, 4 marks (+4) will be awarded to the candidate, and a 1 mark (-1) will be deducted for every incorrect answer.
5. Question papers are available in both English and Hindi.

**1. The set T represents various traversals over a binary tree. The set S represents the order of visiting nodes during a traversal. Which one of the following is the correct match from T to S?**

(A) I - L, II - M, III - N

(B) I - M, II - L, III - N

(C) I - N, II - M, III - L

(D) I - L, II - N, III - M

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**2. Which one of the following options is not a property of Boolean Algebra? (Note: $+$ is OR operation, $\cdot$ is AND operation, and $'$ is NOT operation.)**

(A) $a + b = b + a$

(B) $a \cdot (b + c) = (a \cdot b) + (a \cdot c)$

(C) $a + a = 2a$

(D) $a + (b \cdot c) = (a + b) \cdot (a + c)$

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**3. Which one of the following CPU scheduling algorithms cannot be preemptive?**

(A) Round Robin

(B) Shortest Remaining Time First

(C) First Come First Served

(D) Priority Scheduling

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**4. The keys 5, 28, 19, 15, 26, 33, 12, 17, 10 are inserted into a hash table using the hash function $h(k) = k \mod 9$. The collisions are resolved by chaining. After all the keys are inserted, the length of the longest chain is _____. (answer in integer)**

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**5. Consider the transmission of data bits 110001011 over a link that uses Cyclic Redundancy Check (CRC) code for error detection. If the generator bit pattern is given to be 1001, which one of the following options shows the remainder bit pattern appended to the data bits before transmission?**

(A) 001

(B) 100

(C) 111

(D) 011

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**6. What is the number of clock pulses required to completely load and then unload a 4-bit register?**

(A) 4

(B) 7

(C) 16

(D) 32

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**7. Match the following:**

| | | | |
|---|---|---|---|
| P) | Serial adder | 1) | Combinational Circuit |
| Q) | Parallel Adder | 2) | Sequential Circuit |
| R) | BCD to 7 Segment Decoder | 3) | Neither |
| S) | Priority Encoder | | |

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**8. The state of flip flop when $Q = 0$ and $Q' = 1$**

(A) Reset

(B) Set

(C) Trigger state

(D) Tristate

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**9. Race Around condition can be avoided in Digital logic circuits using?**

(A) Shift Register

(B) Master-Slave JK Flip Flop

(C) Full Adder

(D) AND Gate

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**10. The basic sequential logic building block in which the output follows the data input as long as the ENABLE input is active, is**

(A) J-K flip flop

(B) D flip flop

(C) T flip flop

(D) D latch

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