

CUET PG 2026 Computer Science Question Paper with Solutions

Time Allowed :3 Hours	Maximum Marks :300	Total questions :75
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General Instructions

Read the following instructions very carefully and strictly follow them:

1. The Question Paper consists of 75 Multiple Choice Questions (MCQs).
2. Total marks for the exam is 300.
3. The total duration is 90 minutes; a timer on the screen will display the remaining time, and the exam will automatically submit when the time reaches zero.
4. For every correct answer, 4 marks (+4) will be awarded to the candidate, and a 1 mark (-1) will be deducted for every incorrect answer.
5. Question papers are available in both English and Hindi.

1. The set T represents various traversals over a binary tree. The set S represents the order of visiting nodes during a traversal. Which one of the following is the correct match from T to S?

- (A) I - L, II - M, III - N
- (B) I - M, II - L, III - N
- (C) I - N, II - M, III - L
- (D) I - L, II - N, III - M

Correct Answer: (A) I - L, II - M, III - N

Solution:

Step 1: Understanding the Concept:

Binary tree traversal involves visiting all nodes of a tree in a specific hierarchical order.

Depth-first traversals are categorized based on when the root node is visited relative to its subtrees.

Step 2: Key Formula or Approach:

The standard traversal rules are:

- **Inorder:** Left Subtree → Node → Right Subtree.
- **Preorder:** Node → Left Subtree → Right Subtree.
- **Postorder:** Left Subtree → Right Subtree → Node.

Step 3: Detailed Explanation:

Let's match the sets T and S based on the table provided in the image:

1. **I (Inorder):** The sequence is left subtree, node, then right subtree. This matches with **L**.
2. **II (Preorder):** The sequence starts with the node, followed by the left and right subtrees. This matches with **M**.
3. **III (Postorder):** The sequence visits the subtrees first and the node last. This matches with **N**.

Thus, the correct mapping is I-L, II-M, III-N.

Step 4: Final Answer:

The correct option is (A).

Quick Tip

To remember easily: "Pre", "In", and "Post" refer to the position of the root node. In all three, the Left subtree is always visited before the Right subtree.

2. Which one of the following options is not a property of Boolean Algebra? (Note: + is OR operation, · is AND operation, and ' is NOT operation.)

- (A) $a + b = b + a$
- (B) $a \cdot (b + c) = (a \cdot b) + (a \cdot c)$
- (C) $a + a = 2a$
- (D) $a + (b \cdot c) = (a + b) \cdot (a + c)$

Correct Answer: (C) $a + a = 2a$

Solution:

Step 1: Understanding the Concept:

Boolean Algebra deals with binary variables and logic gates. Unlike standard algebra, it follows specific laws like Idempotent, Commutative, and Distributive laws, where variables can only take values of 0 or 1.

Step 2: Detailed Explanation:

Let's examine each option:

- **Option A:** This is the Commutative Law for addition (OR). It is a valid property.
- **Option B:** This is the Distributive Law where AND distributes over OR. It is a valid property.
- **Option D:** This is the second Distributive Law unique to Boolean Algebra where OR distributes over AND. It is a valid property.
- **Option C:** According to the Idempotent Law, $a + a = a$. In Boolean logic, there is no concept of a coefficient "2" because the result of any logical OR of a variable with itself is simply the variable itself.

Step 3: Final Answer:

The expression $a + a = 2a$ is mathematically incorrect in the context of Boolean Algebra.

Quick Tip

Remember the Idempotent Laws: $x + x = x$ and $x \cdot x = x$. There are no coefficients or exponents in Boolean Algebra.

3. Which one of the following CPU scheduling algorithms cannot be preemptive?

- (A) Round Robin
- (B) Shortest Remaining Time First
- (C) First Come First Served
- (D) Priority Scheduling

Correct Answer: (C) First Come First Served

Solution:

Step 1: Understanding the Concept:

CPU scheduling algorithms are classified as Preemptive or Non-preemptive. In preemptive scheduling, the OS can interrupt a running process to allocate the CPU to another. In non-preemptive scheduling, a process keeps the CPU until it terminates or switches to a waiting state.

Step 2: Detailed Explanation:

- **Round Robin:** Inherently preemptive as it uses time quantum.
- **Shortest Remaining Time First (SRTF):** This is the preemptive version of Shortest Job First (SJF).
- **Priority Scheduling:** Can be either preemptive or non-preemptive.
- **First Come First Served (FCFS):** This is a strictly non-preemptive algorithm. Once the CPU is allocated to a process, it cannot be taken back until the process completes its burst.

Step 3: Final Answer:

FCFS is always non-preemptive.

Quick Tip

FCFS is the simplest scheduling algorithm but often suffers from the "Convoy Effect," where small processes wait behind a very long process.

4. The keys 5, 28, 19, 15, 26, 33, 12, 17, 10 are inserted into a hash table using the hash function $h(k) = k \text{ mod } 9$. The collisions are resolved by chaining. After all the keys are inserted, the length of the longest chain is (answer in integer)

Correct Answer: 3

Solution:

Step 1: Understanding the Concept:

Chaining is a collision resolution technique where each cell of the hash table points to a linked list of records that have the same hash value. The length of a chain is the number of elements in that specific bucket.

Step 2: Key Formula or Approach:

Calculate the remainder for each key using $k \bmod 9$.

Step 3: Detailed Explanation:

Let's compute the hash values for all keys:

- $5 \bmod 9 = 5$
- $28 \bmod 9 = 1$
- $19 \bmod 9 = 1$
- $15 \bmod 9 = 6$
- $26 \bmod 9 = 8$
- $33 \bmod 9 = 6$
- $12 \bmod 9 = 3$
- $17 \bmod 9 = 8$
- $10 \bmod 9 = 1$

Grouping keys by their hash values:

- **Index 1:** {28, 19, 10} → Length = 3
- **Index 3:** {12} → Length = 1
- **Index 5:** {5} → Length = 1
- **Index 6:** {15, 33} → Length = 2
- **Index 8:** {26, 17} → Length = 2

The maximum length observed is 3 at index 1.

Step 4: Final Answer:

The length of the longest chain is 3.

Quick Tip

To solve this quickly, just count the frequency of each remainder. The highest frequency value is your answer.

5. Consider the transmission of data bits 110001011 over a link that uses Cyclic Redundancy Check (CRC) code for error detection. If the generator bit pattern is given

to be 1001, which one of the following options shows the remainder bit pattern appended to the data bits before transmission?

- (A) 001
- (B) 100
- (C) 111
- (D) 011

Correct Answer: (B) 100

Solution:

Step 1: Understanding the Concept:

CRC uses polynomial division where bits are treated as coefficients. To find the CRC remainder, we append $(n - 1)$ zeros to the data (where n is the length of the generator) and perform binary (XOR) division.

Step 2: Key Formula or Approach:

Generator = 1001 (length 4).

Append $4 - 1 = 3$ zeros to the data bits: 110001011**000**.

Step 3: Detailed Explanation:

Perform binary division (XOR subtraction):

$$110001011000 \div 1001$$

$$1100 \oplus 1001 = 0101 \rightarrow \text{bring down } 0 : 1010$$

$$1010 \oplus 1001 = 0011 \rightarrow \text{bring down } 1 : 0111 \text{ (skip leading 0)} \rightarrow \text{bring down } 0 : 1110$$

$$1110 \oplus 1001 = 0111 \rightarrow \text{bring down } 1 : 1111$$

$$1111 \oplus 1001 = 0110 \rightarrow \text{bring down } 1 : 1101$$

$$1101 \oplus 1001 = 0100 \rightarrow \text{bring down } 0 : 1000$$

$$1000 \oplus 1001 = 0001 \rightarrow \text{bring down } 0 : 0010 \rightarrow \text{bring down } 0 : 0100 \text{ (no more bits)}$$

$$\text{Remainder} = 100$$

Step 4: Final Answer:

The remainder is 100, which is option (B).

Quick Tip

In CRC XOR division, you only perform the XOR operation if the leftmost bit of the current dividend is 1. If it is 0, you simply shift to the next bit.

6. What is the number of clock pulses required to completely load and then unload a 4-bit register?

- (A) 4
- (B) 7
- (C) 16
- (D) 32

Correct Answer: (B) 7

Solution:

Step 1: Understanding the Concept:

A serial-in serial-out (SISO) shift register loads bits one by one. To "completely load" means filling all n flip-flops. To "unload" means shifting all stored bits out through the output terminal.

Step 2: Detailed Explanation:

1. To load n bits into an n -bit register, it takes n clock pulses. For a 4-bit register, loading takes 4 pulses.
2. After the 4th pulse, the first bit is already at the output.
3. To shift out the remaining $(n - 1)$ bits, we need $(n - 1)$ more pulses.
4. Total pulses = $n + (n - 1) = 4 + 3 = 7$.

Step 3: Final Answer:

The total clock pulses required is 7.

Quick Tip

General formula for SISO register: Time to load is n cycles. Time to unload (starting after load) is $n - 1$ cycles. Total $2n - 1$.

7. Match the following:

P)	Serial adder	1)	Combinational Circuit
Q)	Parallel Adder	2)	Sequential Circuit
R)	BCD to 7 Segment Decoder	3)	Neither
S)	Priority Encoder		

Correct Answer: P-2, Q-1, R-1, S-1

Solution:

Step 1: Understanding the Concept:

- **Combinational Circuits:** Output depends only on current inputs. No memory elements.
- **Sequential Circuits:** Output depends on current inputs and previous states. Uses memory (flip-flops).

Step 2: Detailed Explanation:

- **P) Serial Adder:** Adds bits bit-by-bit over time. It requires a flip-flop to store the carry for the next bit addition. Thus, it is a **Sequential Circuit (2)**.
- **Q) Parallel Adder:** Adds all bits of a word simultaneously using logic gates. No memory is needed. Thus, it is a **Combinational Circuit (1)**.
- **R) BCD to 7 Segment Decoder:** Converts a 4-bit BCD input to 7 output signals to drive a display. It is a **Combinational Circuit (1)**.
- **S) Priority Encoder:** Encodes inputs based on priority using purely logic gates. It is a **Combinational Circuit (1)**.

Step 3: Final Answer:

The correct match is P-2, Q-1, R-1, S-1.

Quick Tip

Any operation labeled "Serial" typically requires a clock and memory, making it sequential. "Parallel" versions of the same operation are usually combinational.

8. The state of flip flop when $Q = 0$ and $Q' = 1$

- (A) Reset
- (B) Set
- (C) Trigger state
- (D) Tristate

Correct Answer: (A) Reset

Solution:

Step 1: Understanding the Concept:

Flip-flops are bistable devices with two complementary outputs, Q and Q' . The state of the flip-flop is defined by the value of Q .

Step 2: Detailed Explanation:

- When $Q = 1$ (and consequently $Q' = 0$), the flip-flop is in the **Set** state.
- When $Q = 0$ (and consequently $Q' = 1$), the flip-flop is in the **Reset** (or Clear) state.

In the given condition, $Q = 0$, which corresponds to the Reset state.

Step 3: Final Answer:

The state is Reset.

Quick Tip

State is always synonymous with the value of Q . $Q = 0$ means Reset, $Q = 1$ means Set.

9. Race Around condition can be avoided in Digital logic circuits using?

- (A) Shift Register

- (B) Master-Slave JK Flip Flop
- (C) Full Adder
- (D) AND Gate

Correct Answer: (B) Master-Slave JK Flip Flop

Solution:

Step 1: Understanding the Concept:

The Race Around condition occurs in JK flip-flops when $J = 1$, $K = 1$, and the clock pulse width is larger than the propagation delay of the gates. This causes the output to toggle multiple times during a single clock pulse, leading to an unpredictable final state.

Step 2: Detailed Explanation:

There are three main ways to avoid this:

1. Making the clock pulse width smaller than the propagation delay (practically difficult).
2. Using edge-triggered flip-flops instead of level-triggered ones.
3. Using a **Master-Slave JK flip-flop** configuration, where the state is sampled during one part of the clock pulse and output during another, preventing multiple transitions.

Step 3: Final Answer:

The correct method listed is the Master-Slave JK Flip Flop.

Quick Tip

In a Master-Slave setup, the "Master" is active during the high level of the clock, and the "Slave" transfers the value on the falling edge, ensuring only one change per cycle.

10. The basic sequential logic building block in which the output follows the data input as long as the ENABLE input is active, is

- (A) J-K flip flop
- (B) D flip flop
- (C) T flip flop
- (D) D latch

Correct Answer: (D) D latch

Solution:

Step 1: Understanding the Concept:

A transparent device is one where the output is a direct reflection of the input during the active period of the control signal. Latches are level-triggered, whereas flip-flops are edge-triggered.

Step 2: Detailed Explanation:

- **D Flip-Flop:** Only changes state at the clock edge. Between edges, it maintains its state regardless of input changes.

- **D Latch:** When the Enable (or Clock) signal is high, the output Q follows the input D continuously. If D changes while Enable is high, Q changes with it. This is known as transparency.

Step 3: Final Answer:

The building block described is a D latch.

Quick Tip

Latch = Level-triggered (Transparent).

Flip-Flop = Edge-triggered (Non-transparent).