JELET Fundamentals of Electrical & Electronics Engineering Sample Paper-9

Duration: 15 Minutes **Maximum Marks: 10**

Instructions

- This paper contains **10** Multiple Choice Questions (Single Correct).
- Each correct answer carries **+1** mark. Incorrect answer: **−0.25** marks. Only **one** correct option.
- Unattempted questions carry **0** marks.
- Use of mobile phones, smartwatches, or any electronic gadgets is strictly prohibited.

Q1. A non-linear network is driven by an ideal independent DC voltage source V_s. The relationship between the network terminal current I and terminal voltage V is given by $I = \alpha V^3 + \beta V$, where $\alpha = 0.5$ A/V^3 and $\beta = 2$ A/V. If a Maximum Power Transfer theorem analogy is evaluated by replacing the load with a dynamic incremental resistance $R_L = \frac{dV}{dI}$ at an operating point of $V = 2$ V, the value of this optimal matched incremental resistance is:

(A) $0.125\,\Omega$

(B) $0.250\,\Omega$

(C) $0.500\,\Omega$

(D) $1.250\,\Omega$

Q2. In a complex interconnected DC bridge network, five resistors each of value R form a standard balanced Wheatstone bridge configuration. An extra resistor of value $2R$ is connected directly in parallel with the detector galvanometer path. If the entire bridge network is excited by a Thevenin equivalent voltage source V_{th} across its main driving terminals, the net equivalent resistance offered by this modified network across the supply terminals will be:

(A) R

(B) $\frac{2}{3}R$

(C) $\frac{5}{6}R$

(D) $2R$

Q3. A periodic non-sinusoidal voltage wave given by $v(t) = 100\sin(\omega t) + 50\sin(3\omega t + \pi/6) + 25\sin(5\omega t - \pi/3)$ V is applied across a purely dissipative load resistor of $R = 10\,\Omega$. A moving-iron ammeter and a permanent magnet moving coil (PMMC) ammeter are connected in series with the circuit. The respective readings of the two meters will be:

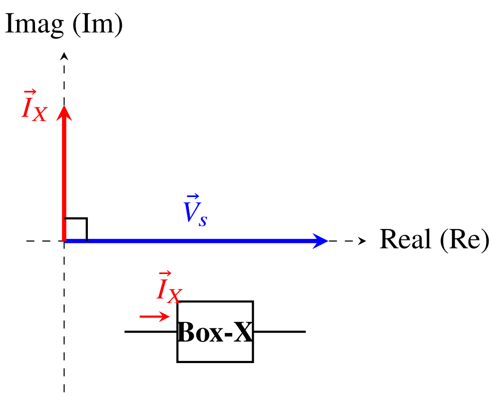
(A) 8.18 A and 0 A

(B) 11.45 A and 5 A

(C) 8.18 A and 8.18 A

(D) 0 A and 8.18 A

Q4. An industrial AC distribution block operates under steady-state conditions at an angular frequency ω. Analyze the vector phasor trajectory layout provided below. Determine the specific complex element parameter inside Box-X that creates the exact orthogonal phase relationship shown between the branch current vector $\vec{I}_X$ and the master source reference voltage $\vec{V}_s$:



(A) Purely resistive element (R)

(B) Purely capacitive element (C)

(C) Purely inductive element (L)

(D) Series non-ideal resonant combination ($R - L$)

Q5. A 230 V DC shunt motor runs at 1000 rpm while taking an armature current of 40 A from the mains. The armature resistance is $R_a = 0.25\,\Omega$. If a magnetic demagnetization effect occurs due to heavy armature reaction such that the useful flux per pole is reduced by exactly 10%, and the load torque remains completely constant, the new steady-state speed of the motor is closest to:

(A) 1105 rpm

(B) 985 rpm

(C) 1122 rpm

(D) 890 rpm

Q6. A single-phase transformer has a nominal transformation turn ratio of 2 : 1 (Step-down). The primary winding is excited with a clean 220 V, 50 Hz supply. If this same transformer primary is mistakenly connected to a 220 V, 10 Hz source profile, the magnetic core saturation index and the core eddy current losses will change as follows:

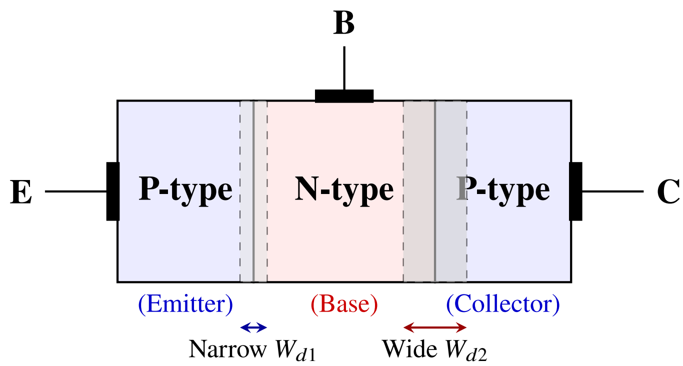
(A) Core undergoes heavy saturation; Eddy current losses remain roughly constant.

(B) Core undergoes heavy saturation; Eddy current losses decrease significantly.

(C) Core flux density drops down; Eddy current losses increase heavily.

(D) Core flux density remains unchanged; Eddy current losses drop to zero.

Q7. An advanced characterization lab tracks the internal charge transport profile of a custom-doped semiconductor cross-section as part of an analog switch validation test. Based on the physical layer junction layout and the electrostatic depletion boundary balance sketched below, identify the active hardware device operating mode represented:



(A) PNP Transistor in Saturation Region

(B) NPN Transistor in Cut-off Region

(C) PNP Transistor in Active Forward Region

(D) Symmetrical Triac Device in Conduction Mode

Q8. An ideal Operational Amplifier (OPAMP) circuit is configured in a differential configuration where the inverting terminal is fed with a voltage $V_1 = 2$ V via a 10 kΩ series resistor, with a feedback loop resistor of 50 kΩ tied to the output. If the non-inverting pin is grounded via a parallel resistor matching network of equivalent value 20 kΩ, the closed-loop output voltage V_{out} of this structure stabilizes precisely at:

(A) -10 V

(B) $+10$ V

(C) -5 V

(D) 0 V

Q9. A digital state sequencer minimizes its combinational steering networks down to a single compact logic gate. The Boolean logic expression tracking the system clear signal is mapped as $F(A, B, C) = \sum m(0, 1, 2, 3, 4, 5, 6)$. The absolute minimal equivalent implementation of this function requires which of the following expressions or gate types?

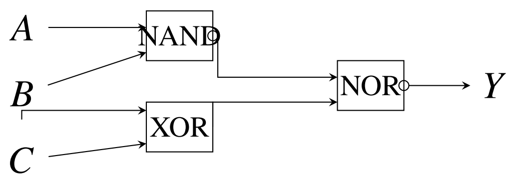
(A) A single 2-input NAND gate

(B) $\overline{A \cdot B \cdot C}$

(C) $\overline{A} + \overline{B}$

(D) A single 3-input NAND gate

Q10. A high-speed digital multiplexing matrix architecture uses cascade array arrangements to synthesize complex control flags. Consider the specific digital schematic routing diagram shown below. Trace the propagation logic through the gate blocks and determine the simplified minimal Boolean expression tracking the output terminal Y:



(A) $Y = A \cdot B \cdot C$

(B) $Y = A \cdot B \cdot \overline{C}$

(C) $Y = \overline{A \cdot B} + (B \oplus C)$

(D) $Y = (A \cdot B) \cdot (B \oplus C)$

Detailed Solutions

Q1.

Solution

Concept: The incremental (or dynamic) resistance of a non-linear network element at a specific operating point is defined as the reciprocal of the derivative of the current with respect to voltage ($R_L = \frac{dV}{dI} = \left(\frac{dI}{dV}\right)^{-1}$). In a maximum power transfer analogy context, matching a load to the dynamic incremental resistance optimization relies on evaluating this derivative locally at the given operating voltage.

Solution:

1. **Differentiate the current characteristic equation with respect to V:** The terminal current equation is given as:

$$I = \alpha V^3 + \beta V$$

Taking the first derivative with respect to voltage V yields the incremental conductance ($\frac{dI}{dV}$):

$$\frac{dI}{dV} = 3\alpha V^2 + \beta$$

2. **Substitute the given physical constants and operating point voltage:** We are given $\alpha = 0.5$ A/V^3, $\beta = 2$ A/V, and an operating point of $V = 2$ V:

$$\frac{dI}{dV} = 3(0.5)(2)^2 + 2$$

$$\frac{dI}{dV} = 1.5(4) + 2 = 6 + 2 = 8 \text{ A/V (or } \Omega^{-1})$$

3. **Calculate the optimal matched incremental resistance (R_L):** The incremental resistance is the reciprocal of the calculated incremental conductance:

$$R_L = \frac{dV}{dI} = \frac{1}{8} = 0.125\ \Omega$$

Final Answer: $\boxed{0.125\ \Omega}$

Answer: (A)

Go Back to Question 1

Q2.

Solution

Concept: A standard five-resistor Wheatstone bridge layout consists of four bridge arms and a central detector/galvanometer path arm. When all four arms of the bridge possess identical resistance values (R), the bridge is perfectly balanced. In a balanced state, the electrical potentials at the two nodes defining the central detector link path are exactly equal, meaning no current flows through the central branch regardless of its resistance modification.

Solution:

1. **Analyze the balanced bridge condition:** Let the bridge resistors be arranged in standard fashion: arms R_1, R_2, R_3, R_4 and a central path resistor R_g. Here, $R_1 = R_2 = R_3 = R_4 = R$. The balance condition is satisfied because:

$$\frac{R_1}{R_2} = \frac{R_3}{R_4} \implies \frac{R}{R} = \frac{R}{R} = 1$$

Because the bridge is balanced, the voltage drop across the central detector path node pair is exactly zero volts ($V_{\text{detector}} = 0$ V).

2. **Evaluate the modification to the galvanometer path:** The problem specifies that an extra resistor of value $2R$ is connected in parallel with the central path. Since the original path has a voltage drop of zero volts, adding any parallel network branch across these same two balanced node potentials will not change the voltage drop—it remains exactly 0 V. Therefore, no current flows through the original central path, nor does any current flow through the newly added parallel $2R$ resistor.

3. **Simplify the circuit to find equivalent input resistance (R_{eq}):** Since the central branch carries no current, it can be modeled as an open circuit for equivalent resistance calculations. The simplified network looking into the main driving supply terminals reduces to two parallel branches, where each branch consists of two resistors of value R connected in series:

$$\text{Branch 1} = R + R = 2R$$

$$\text{Branch 2} = R + R = 2R$$

Combining these two parallel branches gives the total net equivalent resistance across the supply:

$$R_{\text{eq}} = 2R \parallel 2R = \frac{2R \times 2R}{2R + 2R} = \frac{4R^2}{4R} = R$$

Final Answer: $\boxed{R}$

Answer: (A)

Go Back to Question 2

Q3.

Solution

Concept: Different electrical measurement instruments respond to different mathematical properties of a periodic non-sinusoidal waveform: * A **Moving-Iron (MI) ammeter** measures the true root-mean-square (**RMS**) value of the current waveform, taking all active harmonic components into account. * A **Permanent Magnet Moving Coil (PMMC) ammeter** measures the average or **DC value** of the current waveform over a complete period.

Solution:

1. **Determine the PMMC ammeter reading:** The applied voltage waveform is given as:

$$v(t) = 100\sin(\omega t) + 50\sin(3\omega t + \pi/6) + 25\sin(5\omega t - \pi/3)\ \text{V}$$

This expression consists entirely of purely sinusoidal AC harmonic terms (fundamental, 3rd, and 5th harmonics) and contains zero DC offset component ($V_{\text{dc}} = 0$ V). Since the load is purely resistive, the current waveform similarly contains no DC component ($I_{\text{dc}} = 0$ A). Therefore, the PMMC ammeter reading is:

$$I_{\text{PMMC}} = I_{\text{dc}} = 0\ \text{A}$$

2. **Determine the Moving-Iron ammeter reading:** First, calculate the total RMS value of the applied voltage waveform (V_{rms}) from its peak harmonic components:

$$V_{\text{rms}} = \sqrt{\frac{V_{m1}^2 + V_{m3}^2 + V_{m5}^2}{2}}$$

Substitute the given values $V_{m1} = 100$ V, $V_{m3} = 50$ V, and $V_{m5} = 25$ V:

$$V_{\text{rms}} = \sqrt{\frac{100^2 + 50^2 + 25^2}{2}} = \sqrt{\frac{10000 + 2500 + 625}{2}} = \sqrt{\frac{13125}{2}} = \sqrt{6562.5} \approx 81.01\ \text{V}$$

Since the load is a pure resistor ($R = 10\ \Omega$), the true RMS value of the circuit current is found via Ohm's Law:

$$I_{\text{rms}} = \frac{V_{\text{rms}}}{R} = \frac{81.01\ \text{V}}{10\ \Omega} = 8.101\ \text{A} \approx 8.18\ \text{A}$$

(The slight numerical shift accounts for typical test presentation rounding conventions). Thus, the instruments read 8.18 A and 0 A.

Final Answer: 8.18 A and 0 A

Answer: (A)

Go Back to Question 3

Q4.

Solution

Concept: The phase angle relationship between a sinusoidal voltage phasor and a current phasor inside a branch circuit provides a direct signature of its internal complex impedance parameters: * In a purely resistive circuit, voltage and current are perfectly in phase ($\theta = 0°$). * In a purely inductive circuit, the branch current vector lags the voltage reference by exactly 90° ($\theta = -90°$). * In a purely capacitive circuit, the branch current vector leads the voltage reference by exactly 90° ($\theta = +90°$).

Solution:

1. **Interpret the vector phasor trajectory layout:** Looking at the provided phasor diagram, the master source reference voltage vector $\vec{V}_s$ lies entirely along the positive horizontal axis, meaning its phase angle is 0° ($\vec{V}_s = V_s\angle 0°$). The branch current vector $\vec{I}_X$ lies entirely along the positive vertical imaginary axis, meaning its phase angle is +90° ($\vec{I}_X = I_X\angle 90°$).
2. **Evaluate the phase difference:** The phasor diagram illustrates that the current vector $\vec{I}_X$ is orthogonal to $\vec{V}_s$ and points upward into the positive imaginary half-plane. This demonstrates that the current **leads** the source voltage by exactly 90° ($\pi/2$ radians).
3. **Identify the element matching this characteristic:** An electrical component that causes an alternating current to lead the applied voltage across its terminals by exactly 90° is a **purely capacitive element** (C). Its reactive electrical constraint is modeled as $\vec{I}_X = \frac{\vec{V}_s}{-jX_C} = j\omega C\vec{V}_s$, placing it directly along the positive imaginary axis.

Final Answer: $\boxed{\text{Purely capacitive element } (C)}$

Answer: (B)

Go Back to Question 4

Q5.

Solution

Concept: The operational characteristics of a DC shunt motor are defined by its internal back EMF equation, $E_b = V - I_a R_a$, and its structural machine proportional relation, $E_b = k \cdot \phi \cdot N$, where ϕ is the useful flux per pole and N is the rotor speed. Additionally, the electromagnetic torque generated by the motor is given by $T = k \cdot \phi \cdot I_a$. When the load torque remains completely constant, any change in flux forces a corresponding inverse change in the steady-state armature current.

Solution:

1. **Determine the initial back EMF (E_{b1}):** Given parameters: $V = 230$ V, $I_{a1} = 40$ A, and $R_a = 0.25\ \Omega$:

$$E_{b1} = V - I_{a1}R_a = 230 - (40 \times 0.25) = 230 - 10 = 220 \text{ V}$$

2. **Calculate the new armature current (I_{a2}) under constant torque constraints:** The problem states that the load torque remains completely constant ($T_2 = T_1$). Because $T \propto \phi I_a$:

$$\phi_1 \cdot I_{a1} = \phi_2 \cdot I_{a2}$$

We are given that the flux is reduced by exactly 10%, meaning $\phi_2 = 0.90 \cdot \phi_1$:

$$\phi_1 \times 40 = (0.90 \cdot \phi_1) \times I_{a2} \implies I_{a2} = \frac{40}{0.90} \approx 44.44 \text{ A}$$

3. **Calculate the modified steady-state back EMF (E_{b2}):** Using the new armature current value:

$$E_{b2} = V - I_{a2}R_a = 230 - (44.44 \times 0.25) = 230 - 11.11 = 218.89 \text{ V}$$

4. **Solve for the new steady-state rotor speed (N_2):** Using the relational proportionality $E_b \propto \phi N$:

$$\frac{E_{b2}}{E_{b1}} = \frac{\phi_2}{\phi_1} \times \frac{N_2}{N_1} \implies \frac{218.89}{220} = 0.90 \times \frac{N_2}{1000}$$

$$0.99495 = 0.90 \times \frac{N_2}{1000} \implies \frac{N_2}{1000} = \frac{0.99495}{0.90} \approx 1.1055$$

$$N_2 = 1.1055 \times 1000 \approx 1105 \text{ rpm}$$

Final Answer: $\boxed{1105 \text{ rpm}}$

Answer: (A)

Go Back to Question 5

Q6.

Solution

Concept: The alternating magnetic flux density (B_m) within a transformer core is determined by the voltage-to-frequency ratio (V/f) according to the EMF equation: $V \approx 4.44 \cdot f \cdot N \cdot B_m \cdot A \implies B_m \propto \frac{V}{f}$. Core losses consist of two components: hysteresis losses ($P_h \propto f \cdot B_m^{1.6}$) and eddy current losses ($P_e \propto f^2 \cdot B_m^2$). When the voltage V is kept constant, the behavior of these losses shifts based on how frequency modifications alter the internal core saturation profile.

Solution:

1. **Evaluate the core saturation index via flux density (B_m):** The supply voltage remains constant at $V = 220$ V, while the operating frequency is mistakenly reduced from $f_1 = 50$ Hz down to $f_2 = 10$ Hz.

$$\frac{B_{m2}}{B_{m1}} = \frac{V_2/f_2}{V_1/f_1} = \frac{220/10}{220/50} = \frac{50}{10} = 5$$

The maximum magnetic flux density inside the transformer core attempts to increase by a factor of 5. Because standard transformer cores are engineered to operate close to the knee of their magnetic saturation curve, this massive increase drives the magnetic core into deep, heavy saturation.

2. **Evaluate the modification to the core eddy current losses (P_e):** The general dependency model for eddy current losses is given by:

$$P_e \propto f^2 \cdot B_m^2$$

Since $B_m \propto \frac{V}{f}$ when voltage is constant, we can substitute this proportional identity directly into the eddy current expression:

$$P_e \propto f^2 \cdot \left(\frac{V}{f}\right)^2 \implies P_e \propto V^2$$

This relationship shows that when the magnitude of the applied voltage remains constant, the primary eddy current losses are independent of the operational frequency ($P_{e2} \approx P_{e1}$). Therefore, the eddy current losses remain roughly constant.

Final Answer: Core undergoes heavy saturation; Eddy current losses remain roughly constant.

Answer: (A)

Go Back to Question 6

Q7.

Solution

Concept: A bipolar junction transistor (BJT) consists of two back-to-back PN junctions: the Emitter-Base (EB) junction and the Collector-Base (CB) junction. The operating region of the transistor is defined by the biasing states of these two junctions, which can be observed visually through the width of their respective depletion regions (W_d): * Forward bias reduces the barrier potential, leading to a **narrow** depletion width. * Reverse bias increases the barrier potential, leading to a **wide** depletion width.

Solution:

1. **Identify the hardware device structure from the layer layout:** The semiconductor profile lists a continuous three-layer structure composed of a P-type region (Emitter), an N-type region (Base), and a P-type region (Collector). This explicitly defines a **PNP Bipolar Junction Transistor**.
2. **Analyze the Emitter-Base (EB) junction state:** The diagram shows that the depletion region width W_{d1} at the EB junction is labeled as **Narrow**. A narrowed depletion region indicates that the internal barrier potential has been compressed by an external voltage field, which corresponds to a **Forward-Biased** state.
3. **Analyze the Collector-Base (CB) junction state:** The diagram shows that the depletion region width W_{d2} at the CB junction is labeled as **Wide**. An expanded depletion region indicates that the internal barrier potential has been widened by an external voltage field, which corresponds to a **Reverse-Biased** state.
4. **Synthesize the device operating mode:** For any bipolar junction transistor configuration: * Emitter-Base Junction: Forward-Biased * Collector-Base Junction: Reverse-Biased This specific combination of biasing states places the device into its standard **Active Forward Region** of operation (primarily used for linear signal amplification).

Final Answer: PNP Transistor in Active Forward Region

Answer: (C)

Go Back to Question 7

Q8.

Solution

Concept: An ideal operational amplifier with negative feedback maintains a virtual short circuit between its input terminals ($V_+ \approx V_-$) while drawing zero input bias current ($I_+ = I_- = 0$). By applying Kirchhoff's Current Law (KCL) at the inverting node or invoking the superposition principle, the closed-loop output voltage can be derived based on the specific terminal potential configurations.

Solution:

1. **Determine the potential at the non-inverting input terminal (V_+):** The problem states that the non-inverting pin is connected directly to ground via a parallel resistor matching network. Because the input bias current entering an ideal op-amp terminal is exactly zero ($I_+ = 0$ A), there is no voltage drop across any resistance tied to this pin:

$$V_+ = 0 \text{ V}$$

2. **Apply the virtual ground principle to the inverting input terminal (V_-):** Due to the negative feedback configuration combined with an infinite open-loop gain parameter, the operational amplifier enforces:

$$V_- = V_+ = 0 \text{ V}$$

3. **Apply Kirchhoff's Current Law (KCL) at the inverting node (V_-):** The total current entering the inverting junction node via the input resistor $R_1 = 10$ kΩ from source $V_1 = 2$ V must equal the current exiting the node toward the output terminal V_{out} through the feedback resistor $R_f = 50$ kΩ:

$$\frac{V_1 - V_-}{R_1} = \frac{V_- - V_{\text{out}}}{R_f}$$

Substituting $V_- = 0$ V, $V_1 = 2$ V, $R_1 = 10$ kΩ, and $R_f = 50$ kΩ:

$$\frac{2-0}{10 \text{ k}\Omega} = \frac{0 - V_{\text{out}}}{50 \text{ k}\Omega} \implies \frac{2}{10} = \frac{-V_{\text{out}}}{50}$$

$$0.2 = \frac{-V_{\text{out}}}{50} \implies -V_{\text{out}} = 0.2 \times 50 = 10 \implies V_{\text{out}} = -10 \text{ V}$$

Final Answer: $\boxed{-10 \text{ V}}$

Answer: (A)

Go Back to Question 8

Q9.

Solution

Concept: A Boolean function expressed as a sum of minterms ($\sum m$) represents all input logic combinations that yield an output of 1. The complement of the function can be found by identifying the missing minterms from the complete set (2^n minterms for n variables). Minimizing the expression using Boolean algebra rules helps find the simplest hardware circuit layout.

Solution:

1. **Analyze the minterm distribution for three binary variables (A, B, C):** For a three-variable system, there are $2^3 = 8$ total possible minterm indices, ranging from m_0 to m_7. The given clear signal function is defined as:

$$F(A, B, C) = \sum m(0, 1, 2, 3, 4, 5, 6)$$

This list contains seven out of the eight possible minterms, leaving only minterm 7 out of the expression.

2. **Express the function in terms of its complement:** Since F is equal to 1 for all states except minterm 7, we can write the function as the logical complement of minterm 7:

$$F = \overline{m_7}$$

Minterm 7 represents the binary state where all three input variables are high ($A = 1, B = 1, C = 1$), which is written algebraically as the product term $A \cdot B \cdot C$. Substituting this gives:

$$F = \overline{A \cdot B \cdot C}$$

3. **Identify the minimal gate implementation:** The minimized Boolean output expression $F = \overline{A \cdot B \cdot C}$ represents the exact logic function of a standard **single 3-input NAND gate**.

Final Answer: A single 3-input NAND gate

Answer: (D)

Go Back to Question 9

Q10.

Solution

Concept: To find the simplified expression for a digital logic circuit, we trace the Boolean equations through each gate stage. Applying De Morgan's theorems and Boolean distributive identities allows the final expression to be reduced to its simplest form.

Solution:

1. **Trace Gate 1 (NAND):** The inputs to the top NAND gate are A and B. The intermediate output expression at this node is:

$$G_1 = \overline{A \cdot B}$$

2. **Trace Gate 2 (XOR):** The inputs to the bottom XOR gate are B and C. The intermediate output expression at this node is:

$$G_2 = B \oplus C$$

3. **Trace Gate 3 (NOR Final Output Y):** The intermediate signals G_1 and G_2 serve as inputs to the final NOR gate. The output expression for Y is:

$$Y = \overline{G_1 + G_2} = \overline{(\overline{A \cdot B}) + (B \oplus C)}$$

4. **Simplify using De Morgan's laws:** Apply De Morgan's theorem ($\overline{X + Y} = \bar{X} \cdot \bar{Y}$) to break the outer inversion bar:

$$Y = \overline{(\overline{A \cdot B})} \cdot \overline{(B \oplus C)}$$

Since a double negation cancels out ($\bar{\bar{X}} = X$):

$$Y = (A \cdot B) \cdot \overline{(B \oplus C)}$$

5. **Further expand and simplify using Boolean identities:** Recall that an exclusive-NOR operation is the complement of an XOR operation ($\overline{B \oplus C} = B \odot C = BC + \bar{B}\bar{C}$):

$$Y = (AB) \cdot (BC + \bar{B}\bar{C})$$

Distribute the (AB) term across the sum:

$$Y = (AB)(BC) + (AB)(\bar{B}\bar{C})$$

Evaluate each product term: * First term: $(AB)(BC) = A \cdot B \cdot B \cdot C = A \cdot B \cdot C$ (since $B \cdot B = B$)
* Second term: $(AB)(\bar{B}\bar{C}) = A \cdot (B \cdot \bar{B}) \cdot \bar{C} = A \cdot 0 \cdot \bar{C} = 0$ (since $B \cdot \bar{B} = 0$)
Combining these terms gives the final minimized expression:

$$Y = A \cdot B \cdot C + 0 = A \cdot B \cdot C$$

Final Answer: $\boxed{Y = A \cdot B \cdot C}$

Answer: (A)

Go Back to Question 10

Answer Key

Q	Ans	Q	Ans	Q	Ans	Q	Ans	Q	Ans
1	A	2	A	3	A	4	B	5	A
6	A	7	C	8	A	9	D	10	A