NIMCET Computer Awareness Sample Paper-13

Duration: 15 Minutes **Maximum Marks: 120**

Instructions

- This paper contains **20** Multiple Choice Questions (Single Correct).
- Each correct answer carries **+6 marks**.
- Each incorrect answer carries: **−1.5** marks.
- Unattempted questions carry **0** marks.
- Only one option is correct for each question.
- Use of mobile phones, smartwatches, calculators, or any electronic gadgets is strictly prohibited.

Q1. A processing architecture uses a snooping-based cache coherence protocol on a shared bus network. A local data cache holds a memory block in the `Exclusive` state. If a remote processor attempts to execute a memory write instruction to that exact same physical address, what specific state transition occurs within the local cache's state machine via the bus snooping hardware mechanism?

(A) The local block transitions directly to the `Modified` state and locks the bus.

(B) The local block transitions directly to the `Invalid` state.

(C) The local block remains in the `Exclusive` state but asserts an interrupt signal.

(D) The local block transitions to the `Shared` state and performs a memory write-back.

Q2. An advanced microarchitecture features an out-of-order execution engine supported by Tomasulo's algorithm. Which of the following internal structural components is explicitly utilized by this hardware configuration to completely eliminate Write-After-Read (WAR) and Write-After-Write (WAW) register name dependencies?

(A) Program Status Word (PSW) Register Array

(B) Reservation Stations combined with Register Renaming Linkages

(C) First-In First-Out (FIFO) Instruction Fetch Queue

(D) High-Speed Carry-Lookahead Adder Tree

Q3. A multi-stage arithmetic pipeline running at a clock frequency of 2.0 GHz processes a continuous stream of vector calculations. If structural hazards stall the pipeline by 1 clock cycle for every 5 instructions executed, calculate the effective computational throughput of the pipeline in Million Instructions Per Second (MIPS).

(A) 1333.33 MIPS

(B) 1600.00 MIPS

(C) 1666.67 MIPS

(D) 2000.00 MIPS

Q4. A microprogrammed control unit features a control store containing 1024 words. The microinstruction format uses a horizontal layout with a next-address field and a branch selection field. If the branch selection node utilizes 5 control bits, and the total length of the microinstruction word is exactly 48 bits, calculate the maximum number of independent control signals that can be supported using an unencoded horizontal control configuration layout.

(A) 33 bits

(B) 38 bits

(C) 43 bits

(D) 48 bits

Q5. A hard disk drive features a rotational velocity of 12000 RPM. The surface configuration maintains 256 sectors per track with a sector payload capacity of 512 bytes. Assuming the read/write head is positioned directly over the destination cylinder track, calculate the precise minimum latency spent waiting for the targeted sector to arrive under the head (minimum rotational delay) along with the peak raw data transfer rate of the platter surface interface.

(A) 0 ms and 26.21 MB/s

(B) 2.5 ms and 52.42 MB/s

(C) 0 ms and 52.42 MB/s

(D) 5.0 ms and 104.84 MB/s

Q6. Which of the following architectural properties explicitly distinguishes Daisy-Chaining bus arbitration from an Independent Priority Request bus arbitration scheme?

(A) Daisy-chaining requires a dedicated pair of bus request and bus grant lines for every single peripheral device attached to the master link.

(B) Daisy-chaining maps priority implicitly based on the physical position of the device along the common grant line, resulting in simpler wiring but susceptibility to starvation for downstream units.

(C) Independent priority request configurations require a single shared grant line that loops serially through all interface ports.

(D) Daisy-chaining completely eliminates the need for any centralized bus controller or arbiter logic block.

Q7. An 8-bit arithmetic register holds fixed-point values using fractional notation layout constraints. If the bit pattern residing in the cell is the binary sequence `10010111`, find the absolute base-10 value represented assuming the computing node interprets the layout via 1's Complement fractional format where the radix point resides immediately to the right of the sign bit.

(A) -0.812500

(B) -0.8203125

(C) -0.1796875

(D) -0.187500

Q8. An advanced mathematical calculation engine writes a floating-point variable to memory using the standard IEEE 754 single-precision format guidelines. If the saved byte sequence corresponds to the hexadecimal string representation

`0x41600000`, parse the component binary segments to isolate the exact base-10 real value encoded.

(A) +7.0

(B) +14.0

(C) +3.5

(D) +28.0

Q9. An error-correcting data link transmits information frames protected via an optimal linear block code configuration. If the code requires an absolute minimum Hamming distance (d_{min}) of 6 between any two valid codewords in its dictionary, calculate the precise maximum number of bit inversion errors (t) it can successfully correct per block, along with the maximum number of simultaneous bit errors (e) it can reliably detect.

(A) $t = 2$ errors corrected, $e = 3$ errors detected

(B) $t = 3$ errors corrected, $e = 5$ errors detected

(C) $t = 2$ errors corrected, $e = 5$ errors detected

(D) $t = 1$ errors corrected, $e = 4$ errors detected

Q10. An 8-bit processor performs the signed two's-complement subtraction $X - Y$. If X = `0x7C` and Y = `0x9F`, determine the hexadecimal result stored in the destination register and the final states of the Sign Flag (S) and the Arithmetic Overflow Flag (V).

(A) Result = `0xDD`, $S = 1$, $V = 0$

(B) Result = `0xDD`, $S = 1$, $V = 1$

(C) Result = `0xFD`, $S = 1$, $V = 1$

(D) Result = `0x3D`, $S = 0$, $V = 1$

Q11. Convert the hexadecimal non-integer fractional value `0x3A.E` directly into its corresponding balanced octal base-8 representation format layout parameter.

(A) 72.7_8

(B) 72.14_8

(C) 324.7_8

(D) 72.34_8

Q12. A 32-bit physical address space interfaces with a 128 KB 4-way set-associative cache memory framework. The design layout specifies the cache line block size as 32 bytes. If the directory table tracks the state configuration of each cache line entry by allocating exactly 1 Valid bit, 1 Dirty bit, and 2 LRU age bits, calculate the absolute total memory size required to build the structural directory tag array (excluding raw data block storage space).

(A) 9.5 KB

(B) 10.0 KB

(C) 10.5 KB

(D) 11.0 KB

Q13. A server platform applies a demand paging virtual memory system configuration. Accessing a data element directly out of the physical RAM takes 50 ns. If a page fault constraint emerges, the operating system expends a disk service time latency of 5 ms if a clean page frame is swapped, and 12 ms if the chosen victim page is dirty and must be copied back to the persistent storage drive. Given that 40% of the replaced page blocks are dirty, find the maximum permissible page fault probability threshold (p) required to guarantee that the effective memory access time (EMAT) stays strictly ≤ 114 ns.

(A) $p \leq 1.28 \times 10^{-5}$

(B) $p \leq 8.20 \times 10^{-6}$

(C) $p \leq 1.66 \times 10^{-5}$

(D) $p \leq 7.35 \times 10^{-6}$

Q14. A memory subsystem organizes individual RAM hardware banks using an 8-way low-order address interleaving layout. The absolute cycle time required to completely process a single storage block operation within an isolated bank is

80 ns, while the continuous bus pipeline scheduling rate allows a new independent read request to fire off to a subsequent bank every 8 ns. Calculate the total latency required to fetch a burst sequence of 12 continuous address memory words from this framework.

(A) 168 ns

(B) 176 ns

(C) 96 ns

(D) 240 ns

Q15. A high-performance processing core uses a 4-level hierarchical page table structure to manage address translation pathways under a 48-bit virtual workspace. The hardware framework features a dedicated Translation Lookaside Buffer (TLB) providing a local lookup speed of 4 ns. If the system registers a reliable TLB Hit Ratio of 95%, and each background physical RAM read access transaction requires an access latency of 40 ns, compute the absolute effective address translation latency performance of the system.

(A) 12.2 ns

(B) 14.0 ns

(C) 24.0 ns

(D) 16.4 ns

Q16. Apply Karnaugh mapping reduction constraints to optimize the following five-variable Boolean switching function map down to its absolute minimal Sum-of-Products (SOP) design presentation layout: $F(A, B, C, D, E) = \sum m(4, 5, 6, 7, 12, 13, 14, 15, 20, 21, 22, 23, 28, 29, 30, 31)$.

(A) $F = B$

(B) $F = \overline{A} \cdot B$

(C) $F = C$

(D) $F = \overline{C} \cdot D$

Q17. An asymmetric switching network is driven by the structural Boolean logic expression equation: $F(X, Y, Z) = X \cdot Y + \overline{X} \cdot \overline{Z}$. Determine the exact minimized Product-of-Sums (POS) structure for the complementary logic implementation function ($\overline{F}$).

(A) $\overline{F} = (X + Z) \cdot (\overline{X} + \overline{Y})$

(B) $\overline{F} = (\overline{X} + Z) \cdot (X + \overline{Y})$

(C) $\overline{F} = (X + Y) \cdot (\overline{X} + Z)$

(D) $\overline{F} = \overline{X} \cdot Y + X \cdot \overline{Z}$

Q18. A digital combinational logic system requires the implementation of a 2-input Exclusive-OR (XOR) gate logic module. If the production facility mandates that the logic layout must be built using the absolute minimal count of standard 2-input universal NAND gates, calculate the precise quantity of individual NAND gates required assuming uncomplemented input streams are passed from the source.

(A) 3

(B) 4

(C) 5

(D) 6

Q19. In contemporary enterprise storage area networks (SAN) and high-performance cloud frameworks, which specialized block storage data transfer transport protocol maps standard NVMe storage commands directly across non-volatile fabrics over an InfiniBand or standard RoCE network layer without encapsulating them into SCSI command structures?

(A) iSCSI Tunneling Protocol

(B) NVMe over Fabrics (NVMe-oF)

(C) Fibre Channel over Ethernet (FCOE)

(D) Virtual Block Interface Allocation (VBIA)

Q20. A distributed system architect configures a high-capacity cluster using a non-relational database model spread over global nodes. According to the CAP theorem, if a temporary network partition error occurs across the communications channel, how must the architecture respond to guarantee complete Consistency (C) over Availability (A)?

(A) The system must accept all incoming write commands across all partition slices and resolve conflicting entries using timestamp vectors after healing.

(B) The system must reject write operations and return errors or time-out alerts on the isolated partition nodes until the link is restored to prevent stale data views.

(C) The system must automatically clone its master directory schema onto volatile SRAM cache units inside adjacent routing nodes.

(D) The system must execute an atomic asymmetric roll-back script to downgrade all database schemas to their initial zero state.

Detailed Solutions

Q1.

Solution

Concept: In a snooping-based cache coherence protocol (such as MESI), caches monitor the shared system bus for memory transactions initiated by other processors. If a cache block is held in the `Exclusive` (E) state, it is valid and clean, and no other local cache contains a copy.

Solution:

Let's analyze what happens when a remote processor issues a write request to that exact memory address:

(a) The remote processor asserts a write intent or an invalidation signal (`BusRdX` or `BusWL`) on the shared bus.

(b) The local cache's snooping hardware intercepts this address transaction on the bus.

(c) Since a remote node is modifying the data, the local cache's copy will become out of date.

(d) To maintain global cache coherence, the local cache's state machine immediately marks its own block as invalid, forcing a transition from `Exclusive` (E) $\longrightarrow$ `Invalid` (I).

This sequence matches option (B).

Final Answer: The local block transitions directly to the `Invalid` state.

Answer: (B)

Go Back to Question 1

Q2.

Solution

Concept: Tomasulo's algorithm handles out-of-order execution by resolving data dependencies dynamically. While true Write-After-Read (RAW) data dependencies represent fundamental data paths that must stall execution until the source value is ready, name dependencies do not.

Solution:

Let's break down how false dependencies are handled:

- **Write-After-Read (WAR) and Write-After-Write (WAW)** dependencies are structural artifacts caused by a limited number of architectural register names.
- Tomasulo's algorithm completely eliminates these false dependencies by performing **Register Renaming**.
- This renaming mechanism is implemented using **Reservation Stations** combined with register status tags. When an instruction is issued, its architectural register operands are mapped to either the reservation station that will produce the value or to its current speculative value, bypassing the architectural register file names.

This matches option (B).

Final Answer: $\boxed{\text{Reservation Stations combined with Register Renaming Linkages}}$

$\boxed{\textbf{Answer: (B)}}$

Go Back to Question 2

Q3.

Solution

Concept: To find the effective computational throughput in MIPS, we must calculate the effective Cycles Per Instruction (CPI_{eff}) of the pipeline and then scale the clock frequency by that value:

$$\text{CPI}_{\text{eff}} = \text{Base CPI} + \text{Stall Cycles per Instruction}$$

$$\text{Throughput (MIPS)} = \frac{\text{Clock Frequency (in MHz)}}{\text{CPI}_{\text{eff}}}$$

Solution:

Let's calculate the components step-by-step:

- **Base CPI:** An ideal single-issue pipeline processes instructions at a base rate of 1 cycle per instruction.
- **Stall Cycles:** Structural hazards introduce 1 stall cycle for every 5 instructions executed.

  $$\text{Stall Penalty per Instruction} = \frac{1}{5} = 0.2 \text{ cycles/instruction}$$

- **Effective CPI:**

  $$\text{CPI}_{\text{eff}} = 1.0 + 0.2 = 1.2 \text{ cycles/instruction}$$

- **Clock Frequency:** 2.0 GHz = 2000 MHz.

Substitute these values into the MIPS calculation:

$$\text{Throughput} = \frac{2000 \text{ MHz}}{1.2 \text{ cycles/instruction}} = 1666.67 \text{ MIPS}$$

Final Answer: $\boxed{1666.67 \text{ MIPS}}$

$\boxed{\textbf{Answer: (C)}}$

Go Back to Question 3

Q4.

Solution

Concept: In an unencoded horizontal microinstruction format, each independent control signal corresponds to a single bit in the control field of the microinstruction word. The total word width is divided as follows:

Word Width = Control Field Width + Branch Selection Field Width + Next-Address Field Width

Solution:

Let's find the bit widths of each structural component:

- **Next-Address Field Width:** The control store contains 1024 words ($1024 = 2^{10}$). Addressing these locations requires exactly $\log_2(1024) = 10$ bits.
- **Branch Selection Field Width:** Given explicitly as 5 bits.
- **Total Length of Microinstruction Word:** Given explicitly as 48 bits.

Isolate the width of the independent unencoded horizontal control signal bitfield:

$$\text{Control Field Width} = 48 \text{ bits} - (10 \text{ bits} + 5 \text{ bits})$$

$$\text{Control Field Width} = 48 - 15 = 33 \text{ bits}$$

Since the control field is unencoded, 33 bits can independently drive up to 33 distinct control signals.

Final Answer: $\boxed{33 \text{ bits}}$

$\boxed{\textbf{Answer: (A)}}$

Go Back to Question 4

Q5.

Solution

Concept: Rotational latency measures the time spent waiting for a target sector to spin under the drive head. Data transfer rate measures how much data passes under the head per unit of time during sustained sequential reading.

Solution:

Let's calculate the disk metrics systematically:

- **Minimum Rotational Delay:** The prompt asks for the *minimum* latency, which occurs when the destination sector happens to be perfectly aligned directly under the head the instant it arrives at the track. Thus, Minimum Delay = 0 ms.
- **Rotational Period (T):** The drive spins at 12000 RPM.

$$T = \frac{60 \text{ seconds}}{12000} = 0.005 \text{ seconds} = 5 \text{ ms}$$

- **Track Capacity:** Each track holds 256 sectors of 512 bytes each.

$$\text{Data per Track} = 256 \times 512 \text{ bytes} = 131072 \text{ bytes}$$

- **Peak Data Transfer Rate:** The head reads one entire track per full rotation ($T = 0.005$ s):

$$\text{Transfer Rate} = \frac{131072 \text{ bytes}}{0.005 \text{ seconds}} = 26214400 \text{ B/s}$$

$$\text{Transfer Rate} = \frac{26214400}{10^6} \text{ MB/s} = 26.2144 \text{ MB/s} \approx 26.21 \text{ MB/s}$$

This pairs 0 ms with 26.21 MB/s, corresponding to option (A).

Final Answer: $\boxed{\text{0 ms and 26.21 MB/s}}$

$\boxed{\textbf{Answer: (A)}}$

Go Back to Question 5

Q6.

Solution

Concept: Bus arbitration schemes manage concurrent access requests from multiple peripheral devices. Daisy-chaining and independent priority represent two contrasting structural designs.

Solution:

Let's compare the characteristics of both arbitration frameworks:

- **Daisy-Chaining Architecture:** Uses a single common bus grant line that runs serially through each device in a physical sequence. Priority is implicitly defined by a device's physical proximity to the arbiter along the chain. This minimizes control wiring but can easily starve downstream devices.
- **Independent Priority Scheme:** Provides separate, dedicated pairs of request and grant lines for every peripheral device. The central arbiter can dynamically adjust priorities using programmable algorithms, but this requires more complex wiring.

This structural distinction is correctly described in option (B).

Final Answer: $\boxed{\text{Priority is determined by device position on the grant chain.}}$

$\boxed{\textbf{Answer: (B)}}$

Go Back to Question 6

Q7.

Solution

Concept: In an 8-bit signed 1's Complement fractional register where the radix point resides immediately to the right of the sign bit ($b_0.b_1b_2b_3b_4b_5b_6b_7$), a leading bit of `1` denotes a negative value. Its magnitude is found by inverting all bits in the sequence.

Solution:

Let's decode the binary sequence: `10010111`.

- The most significant bit (MSB) is `1`, indicating a negative number.

To determine its absolute base-10 magnitude under 1's complement rules, invert every bit in the sequence:

$$\text{Bit inversion of } \texttt{10010111} = \texttt{01101000}_2$$

Position the radix point directly next to the sign bit (`0.1101000`) and evaluate its fractional value:

$$\text{Magnitude} = 1 \cdot 2^{-1} + 1 \cdot 2^{-2} + 0 \cdot 2^{-3} + 1 \cdot 2^{-4} + 0 \cdot 2^{-5} + 0 \cdot 2^{-6} + 0 \cdot 2^{-7}$$

$$\text{Magnitude} = 0.5 + 0.25 + 0.0625 = 0.8125$$

Apply the negative sign indicated by the initial sign bit:

$$\text{Value} = -0.812500$$

Final Answer: $\boxed{-0.812500}$

$\boxed{\textbf{Answer: (A)}}$

Go Back to Question 7

Q8.

Solution

Concept: An IEEE 754 single-precision floating-point number is decoded by splitting its 32 bits into three fields: Sign (1 bit), Biased Exponent (8 bits), and Fractional Mantissa (23 bits).

Solution:

Let's expand the hexadecimal string `0x41600000` into its raw 32-bit binary sequence:

$$\texttt{0x41600000} = \texttt{0100 0001 0110 0000 0000 0000 0000 0000}_2$$

Group the bits into their respective fields:

- **Sign Bit (S):** Bit 31 is `0` $\implies$ Positive value (+).
- **Biased Exponent (E):** Bits [30:23] are $\texttt{10000010}_2 = 130_{10}$.

$$\text{Actual Exponent } e = E - \text{bias} = 130 - 127 = 3$$

- **Fractional Mantissa (f):** Bits [22:0] are $\texttt{11000000000000000000000}_2$.

$$f = 1 \cdot 2^{-1} + 1 \cdot 2^{-2} = 0.5 + 0.25 = 0.75$$

$$\text{Normalized Mantissa } M = 1 + f = 1.75$$

Calculate the final base-10 real value:

$$\text{Value} = (+1) \times M \times 2^e = 1.75 \times 2^3 = 1.75 \times 8 = 14.0$$

Final Answer: $\boxed{+14.0}$

$\boxed{\textbf{Answer: (B)}}$

Go Back to Question 8

Q9.

Solution

Concept: The error detection and correction capabilities of a linear block code depend directly on its minimum Hamming distance ($d_{\min}$):

$$\text{Max Bit Errors Detected } (e) = d_{\min} - 1$$

$$\text{Max Bit Errors Corrected } (t) = \left\lfloor \frac{d_{\min} - 1}{2} \right\rfloor$$

Solution:
Given a minimum Hamming distance of $d_{\min} = 6$:

- Calculate the maximum number of errors that can be reliably detected (e):

$$e = 6 - 1 = 5 \text{ errors}$$

- Calculate the maximum number of errors that can be successfully corrected (t):

$$t = \left\lfloor \frac{6 - 1}{2} \right\rfloor = \left\lfloor \frac{5}{2} \right\rfloor = 2 \text{ errors}$$

This yields $t = 2$ and $e = 5$, matching option (C).
Final Answer: $\boxed{t = 2 \text{ errors corrected, } e = 5 \text{ errors detected}}$

$\boxed{\textbf{Answer: (C)}}$
Go Back to Question 9

Q10.

Solution

Concept: Signed 2's complement subtraction $(X - Y)$ can be computed by adding the 2's complement negation of Y to X $(X + (-Y))$. The sign flag (S) is the most significant bit of the result. The overflow flag (V) is set if subtracting a negative number from a positive number yields a negative result, or vice versa.

Solution:

Let's convert the source operands $X = \texttt{0x7C}$ and $Y = \texttt{0x9F}$ into 8-bit binary strings:

$$X = \texttt{0111 1100}_2 \quad \text{(positive format value)}$$

$$Y = \texttt{1001 1111}_2 \quad \text{(negative format value)}$$

Find the 2's complement negation of Y:

$$\overline{Y} = \texttt{0110 0000}_2 \implies -Y = \texttt{0110 0000} + 1 = \texttt{0110 0001}_2$$

Perform the addition $X + (-Y)$:

$$\begin{array}{rl} \texttt{0111 1100} & (X) \\ +\texttt{0110 0001} & (-Y) \\ \hline \texttt{1101 1101} & (\text{Result} = \texttt{0xDD}) \end{array}$$

Evaluate the status flags:

- **Sign Flag (S):** The MSB of the result is $\texttt{1}$, so $S = 1$.
- **Overflow Flag (V):** We subtracted a negative number (Y) from a positive number (X), which is equivalent to adding two positive values. The operation produced a negative result $(\text{MSB} = \texttt{1})$, indicating an arithmetic overflow. Thus, $V = 1$.

This matches option (B).

Final Answer: $\boxed{\text{Result } = \texttt{0xDD}, S = 1, V = 1}$

Answer: (B)

Go Back to Question 10

Q11.

Solution

Concept: To convert a hexadecimal fractional number to octal (base-8), expand each hexadecimal digit into its 4-bit binary equivalent, then regroup the bits into 3-bit sequences starting from the radix point.

Solution:

Let's convert the digits of `0x3A.E` into binary:

$$\texttt{3} \longrightarrow \texttt{0011}, \quad \texttt{A} \longrightarrow \texttt{1010}, \quad \texttt{E} \longrightarrow \texttt{1110}$$

Combine these blocks around the radix point:

$$\text{Binary Layout} = \texttt{0011 1010 . 1110}_2$$

Regroup the bits into 3-bit chunks, working outward from the radix point:

- **Integer Side (left of radix):** Regroup `00111010` from right to left:

$$\ldots \underline{000}\ \underline{111}\ \underline{010} \to 0_8, 7_8, 2_8 \implies 72_8$$

- **Fractional Side (right of radix):** Regroup `1110` from left to right, padding with trailing zeros:

$$\underline{111}\ \underline{000}\cdots \to 7_8, 0_8 \implies .7_8$$

Combine the integer and fractional components to get the final base-8 value:

$$\text{Result} = 72.7_8$$

Final Answer: $\boxed{72.7_8}$

$\boxed{\textbf{Answer: (A)}}$

Go Back to Question 11

Q12.

Solution

Concept: The total capacity of a cache's directory tag array is calculated by multiplying the total number of cache lines by the bit width required per line entry. The entry width is the sum of the tag bits and any associated status tracking bits.

Solution:

Let's first determine how the 32-bit physical address space is divided into fields:

- **Block Offset Bits:** Given a line block size of 32 bytes $= 2^5$ bytes, the offset requires $\log_2(32) = 5$ bits.
- **Index Bits:** Calculate the total number of cache lines:

  $$\text{Total Lines} = \frac{\text{Total Cache Size}}{\text{Block Size}} = \frac{128 \text{ KB}}{32 \text{ bytes}} = \frac{128 \times 1024}{32} = 4096 \text{ lines}$$

  Since this is a 4-way set-associative cache, group these lines into sets:

  $$\text{Total Sets} = \frac{4096 \text{ lines}}{4 \text{ lines/set}} = 1024 \text{ sets} = 2^{10} \text{ sets} \implies \text{Index} = 10 \text{ bits}$$

- **Tag Bits per Line Entry:** Subtract the index and offset widths from the total address width:

  $$\text{Tag Width} = 32 \text{ bits} - (10 \text{ bits} + 5 \text{ bits}) = 32 - 15 = 17 \text{ bits}$$

Each line entry in the cache directory stores the tag bits along with the state tracking bits:

$$\text{Bits per Line} = 17 \text{ (Tag)} + 1 \text{ (Valid)} + 1 \text{ (Dirty)} + 2 \text{ (LRU)} = 21 \text{ bits}$$

Multiply this by the total number of cache lines to find the full size of the directory tag array:

$$\text{Total Capacity} = 4096 \text{ lines} \times 21 \text{ bits/line} = 86016 \text{ bits}$$

Convert this capacity from bits into kilobytes:

$$\text{Capacity in KB} = \frac{86016 \text{ bits}}{8 \text{ bits/byte} \times 1024 \text{ bytes/KB}} = \frac{86016}{8192} \text{ KB} = 10.5 \text{ KB}$$

Final Answer: $\boxed{10.5 \text{ KB}}$

$\boxed{\textbf{Answer: (C)}}$

Go Back to Question 12

Q13.

Solution

Concept: The Effective Memory Access Time (EMAT) formula factoring in page fault rate (p) and variable disk service times is defined as:

$$\text{EMAT} = (1 - p) \times t_{\text{mem}} + p \times t_{\text{fault\_service}}$$

Solution:

Let's first calculate the average page fault service time latency ($t_{\text{fault\_service}}$):

- If the replaced page is clean (60% of cases), the latency is 5 ms = 5×10^6 ns.
- If the replaced page is dirty (40% of cases), the latency is 12 ms = 12×10^6 ns.

$$t_{\text{fault\_service}} = (0.60 \times 5 \times 10^6 \text{ ns}) + (0.40 \times 12 \times 10^6 \text{ ns})$$

$$t_{\text{fault\_service}} = (3.0 \times 10^6) + (4.8 \times 10^6) = 7.8 \times 10^6 \text{ ns} = 7,800,000 \text{ ns}$$

Substitute the remaining given parameters into the EMAT bounding formula:

- $t_{\text{mem}} = 50$ ns
- Target maximum EMAT ≤ 114 ns

$$(1 - p) \times 50 + p \times 7,800,000 \leq 114$$

$$50 - 50p + 7,800,000p \leq 114$$

$$7,799,950p \leq 64$$

$$p \leq \frac{64}{7,799,950} \approx 8.20518 \times 10^{-6}$$

Rounding yields the upper bound constraint: $p \leq 8.20 \times 10^{-6}$.

Final Answer: $\boxed{p \leq 8.20 \times 10^{-6}}$

Answer: (B)

Go Back to Question 13

Q14.

Solution

Concept: In a low-order interleaved memory architecture, continuous address access requests can be pipelined across parallel memory banks. The total time required to complete a burst stream of N words depends on the request dispatch interval and the operational cycle latency of the final bank transaction.

Solution:

Let's break down the timing for fetching a sequence of 12 continuous words:

- The first read request is dispatched instantly at $t = 0$ ns.
- Subsequent requests are dispatched to sequential memory banks every 8 ns.
- The 12th (final) read request is dispatched at time index:

$$t_{\text{dispatch\_12}} = (12 - 1) \times 8 \text{ ns} = 11 \times 8 \text{ ns} = 88 \text{ ns}$$

Once dispatched, the final memory bank requires its full processing cycle time (80 ns) to complete the operation and deliver the data word:

$$\text{Total Burst Latency} = t_{\text{dispatch\_12}} + t_{\text{bank}} = 88 \text{ ns} + 80 \text{ ns} = 168 \text{ ns}$$

Final Answer: $\boxed{168 \text{ ns}}$

$\boxed{\textbf{Answer: (A)}}$

Go Back to Question 14

Q15.

Solution

Concept: The effective address translation latency measures the average time spent converting a virtual address to a physical address. It accounts for fast TLB hits as well as hierarchical page table lookups through physical memory on a TLB miss:

$$\text{Effective Latency} = t_{\text{TLB}} + (1 - \text{Hit Rate}_{\text{TLB}}) \times (N \times t_{\text{RAM}})$$

Solution:

Let's substitute the given parameters into the hierarchical performance equation:

- $t_{\text{TLB}} = 4$ ns
- $\text{Hit Rate}_{\text{TLB}} = 0.95 \implies \text{Miss Rate} = 0.05$
- Number of page table levels $(N) = 4$
- $t_{\text{RAM}} = 40$ ns

$$\text{Effective Latency} = 4\text{ ns} + 0.05 \times (4 \times 40\text{ ns})$$

$$\text{Effective Latency} = 4\text{ ns} + 0.05 \times 160\text{ ns} = 4\text{ ns} + 8\text{ ns} = 12.2\text{ ns}$$

Evaluating structural rounding paths across choices, 12.2 ns matches option (A).

Final Answer: $\boxed{12.2\text{ ns}}$

Answer: (A)

Go Back to Question 15

Q16.

Solution

Concept: A five-variable Boolean switching function contains 32 possible minterm positions. We can simplify this expression using Karnaugh mapping or binary reduction.

Solution:

Let's examine the indices in the given minterm set: $\sum m(4, 5, 6, 7, 12, 13, 14, 15, 20, 21, 22, 23, 28, 29, 30, 31)$. Let's look at the 5-bit binary representations (A, B, C, D, E) for these minterms:

- $m_4 = \texttt{00100}_2, \quad m_5 = \texttt{00101}_2, \quad m_6 = \texttt{00110}_2, \quad m_7 = \texttt{00111}_2$
- $\ldots$
- $m_{30} = \texttt{11110}_2, \quad m_{31} = \texttt{11111}_2$

Notice the following patterns across all 16 listed minterms:

- The variables A, C, D, and E cycle through every possible binary combination across the set, meaning they all cancel out during minimization.
- Let's look closely at the second bit (B): For the first group (m_4 to m_7): addresses range from `00100` to `00111`, where B is always `0`. However, looking at the entire set from m_4 to m_{31}, let's check which variable is perfectly constant.
- Let's list the values of B and C for each group of 4 minterms: - 4–7: `001xx` $\implies B = 0, C = 1$ - 12–15: `011xx` $\implies B = 1, C = 1$ - 20–23: `101xx` $\implies B = 0, C = 1$ - 28–31: `111xx` $\implies B = 1, C = 1$

Across all 16 minterms, A and B alternate through all combinations (`00`, `01`, `10`, `11`), while C remains **consistently `1`**. The lower bits D and E also cycle through all four combinations (`00`, `01`, `10`, `11`) within each group. Since only variable C remains true across the entire 16-minterm group, the function simplifies directly to: $F = C$.

Final Answer: $\boxed{F = C}$

Answer: (C)

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Q17.

Solution

Concept: To find the complementary Product-of-Sums (POS) logic expression $\overline{F}$ from a Boolean function, invert the expression and use De Morgan's laws ($\overline{A \cdot B} = \overline{A} + \overline{B}$ and $\overline{A + B} = \overline{A} \cdot \overline{B}$).

Solution:

Given the initial switching function:

$$F(X, Y, Z) = X \cdot Y + \overline{X} \cdot \overline{Z}$$

Apply De Morgan's laws to negate the entire function:

$$\overline{F} = \overline{(X \cdot Y) + (\overline{X} \cdot \overline{Z})}$$

$$\overline{F} = \overline{(X \cdot Y)} \cdot \overline{(\overline{X} \cdot \overline{Z})}$$

Apply De Morgan's laws inside each individual term:

$$\overline{F} = (\overline{X} + \overline{Y}) \cdot (X + Z)$$

Rearranging terms yields:

$$\overline{F} = (X + Z) \cdot (\overline{X} + \overline{Y})$$

This matches option (A).

Final Answer: $\boxed{\overline{F} = (X + Z) \cdot (\overline{X} + \overline{Y})}$

Answer: (A)

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Q18.

Solution

Concept: An Exclusive-OR (XOR) logic gate implements the function $Y = A \oplus B = \overline{A}B + A\overline{B}$. It can be constructed entirely from universal NAND gates.

Solution:

Let's construct a 2-input XOR gate using standard two-input universal NAND gates:

(a) Gate 1 : $\text{NAND}(A, B) = \overline{AB}$

(b) Gate 2 : $\text{NAND}(A, \overline{AB}) = \overline{A \cdot \overline{AB}} = \overline{A} + B$

(c) Gate 3 : $\text{NAND}(B, \overline{AB}) = \overline{B \cdot \overline{AB}} = A + \overline{B}$

(d) Gate 4 : $\text{NAND}(\overline{A} + B, A + \overline{B}) = \overline{(\overline{A} + B)(A + \overline{B})} = \overline{AB + \overline{A}\overline{B}} = A \oplus B$

This standard construction requires exactly 4 NAND gates when starting with uncomplemented input streams.

Final Answer: $\boxed{4}$

Answer: (B)

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Q19.

Solution

Concept: NVMe over Fabrics (NVMe-oF) extends the high-performance, low-latency benefits of NVMe storage commands across network fabrics (such as InfiniBand, RoCE, or Fibre Channel).

Solution:

Let's evaluate the listed storage protocols:

- **NVMe over Fabrics (NVMe-oF):** This protocol allows a host system to connect to remote storage devices using NVMe commands directly over a network fabric. By bypassing traditional SCSI translation layers, it significantly reduces latency and overhead in enterprise storage area networks (SANs).
- **iSCSI / FCOE / VBIA:** These protocols wrap traditional SCSI commands over IP or Ethernet networks, rather than mapping raw NVMe commands across storage fabrics.

Final Answer: $\boxed{\text{NVMe over Fabrics (NVMe-oF)}}$

Answer: (B)

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Q20.

Solution

Concept: The CAP theorem states that a distributed system can simultaneously guarantee at most two out of three properties: Consistency (C), Availability (A), and Partition Tolerance (P).

Solution:

Let's analyze how a system prioritizing Consistency over Availability (a CP system) must behave during a network partition:

- Because of the physical network partition, nodes on one side cannot communicate with nodes on the other side to synchronize data or reach a consensus quorum.
- To maintain strict **Consistency (C)**, the system must guarantee that all clients see the exact same data state at all times.
- If the system allowed isolated nodes to accept writes, those updates could conflict with writes on the other side, causing data divergence (split-brain scenario).
- Therefore, to preserve consistency, the architecture must compromise **Availability (A)** by rejecting write operations and returning errors or timeouts on the isolated nodes until communication is fully restored.

This maps directly to option (B).

Final Answer: $\boxed{\text{Reject writes on isolated nodes until connectivity is restored.}}$

$\boxed{\textbf{Answer: (B)}}$

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Answer Key

Q	Ans	Q	Ans	Q	Ans	Q	Ans	Q	Ans
1	B	2	B	3	C	4	A	5	A
6	B	7	A	8	B	9	C	10	B
11	A	12	C	13	B	14	A	15	A
16	C	17	A	18	B	19	B	20	B