Semiconductor Electronics JEE Main PYQ - 1

Total Time: 1 Hour **Total Marks:** 100

Instructions

Instructions

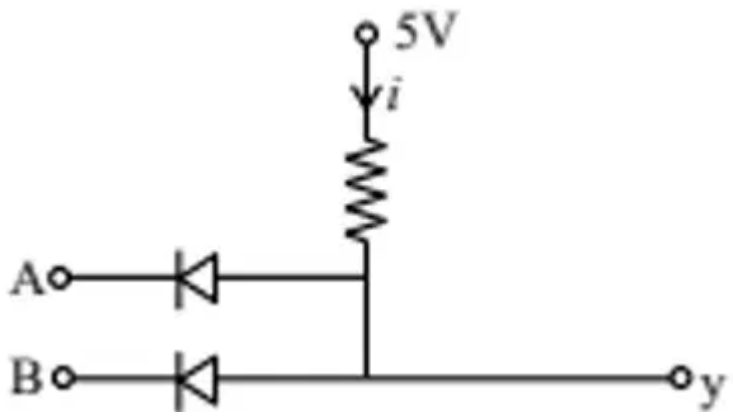
1. Test will auto submit when the Time is up.
2. The Test comprises of multiple choice questions (MCQ) with one or more correct answers.
3. The clock in the top right corner will display the remaining time available for you to complete the examination.

Navigating & Answering a Question

1. The answer will be saved automatically upon clicking on an option amongst the given choices of answer.
2. To deselect your chosen answer, click on the clear response button.
3. The marking scheme will be displayed for each question on the top right corner of the test window.

Semiconductor Electronics

1. For the circuit below, identify the logic gate: **(+4, -1)**



a. AND

b. OR

c. NAND

d. NOR

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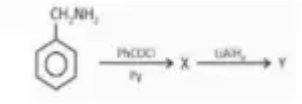
2. Consider the following reaction. **(+4, -1)**



The correct structure of Y is

a. $PhCH_2NHCOPh$

b. Phâ€“CH_2NCH_2Ph

c. $PhNH_2CH_2Ph$

d. $PhCH_3$

---

3. A metallic conductor of length 2m and cross-sectional area $0.2\,\mathrm{mm}^2$ carries a steady current of 1.2 A when a potential difference of 2 V is applied across it. ($e =$ **(+4, -1)**

1.6×10^{-19}, charge density = $7.5 \times 10^{28}\,\mathrm{m}^{-3}$) Then the mobility of the charge carrier is $x \times 10^{-4}$ SI units. Find x.

---

4. For the given statements below, mark the correct option. Statement-I: Work done by a conservative force f, from r_1 to r_2 is given by: **(+4, -1)**

$$W = \int_{r_1}^{r_2} f\, dr.$$

Statement-II: Work done by conservative force is path dependent.

a. Statement-I and Statement-II is true

b. Statement-I is true and Statement-II is false

c. Statement-I is false and Statement-II is true

d. Statement-I and Statement-II is false

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5. Statement-1: Time period of simple pendulum is increased if density of material of pendulum is increased. Statement-2: Time period of simple pendulum is $T = 2\pi\sqrt{\frac{l}{g}}$. **(+4, -1)**

a. Statement I is true; Statement II is true

b. Statement I is true; Statement II is false

c. Statement I is false; Statement II is true

d. Statement I is false; Statement II is false

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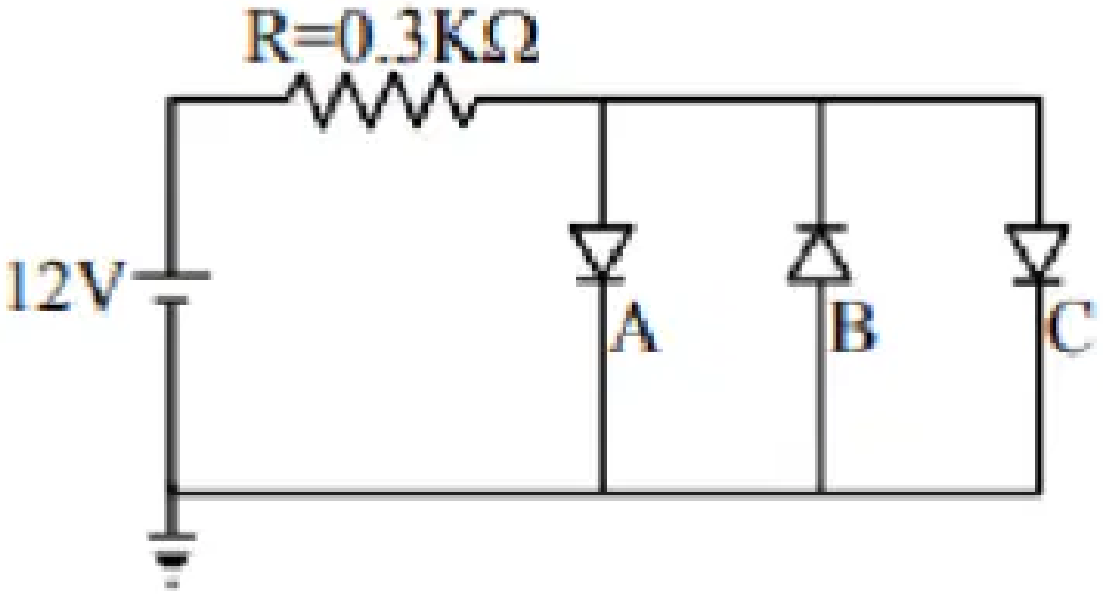
6. Three silicon diodes connected parallel to each other as shown. Forward voltage of diode is 0.7 V. Find current through diode A : **(+4, -1)**



a. $\frac{113}{3}$ mA

b. $\frac{113}{6}$ mA

c. $\frac{113}{9}$ mA

d. $\frac{226}{3}$ mA

---

7. A zener diode of breakdown voltage 10 V is connected to an external voltage of 15 V and a resistance R in series. If power of zener diode is 0.4 W. Find value of unknown resistance R : (+4, -1)

a. 125 Ω

b. 105 Ω

c. 130 Ω

d. 115 Ω

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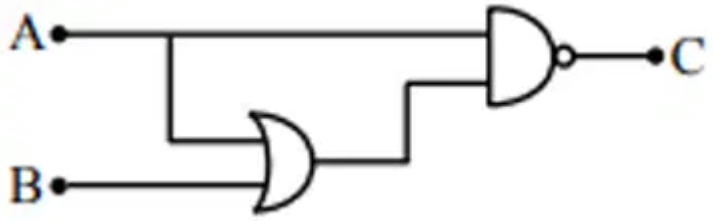
8. For given logic gate circuit choose correct truth table. (+4, -1)



a.

A	B	C
0	0	1
1	0	1
0	1	1
1	1	0

b.

A	B	C
0	0	1
1	0	0
0	1	1
1	1	0

c.

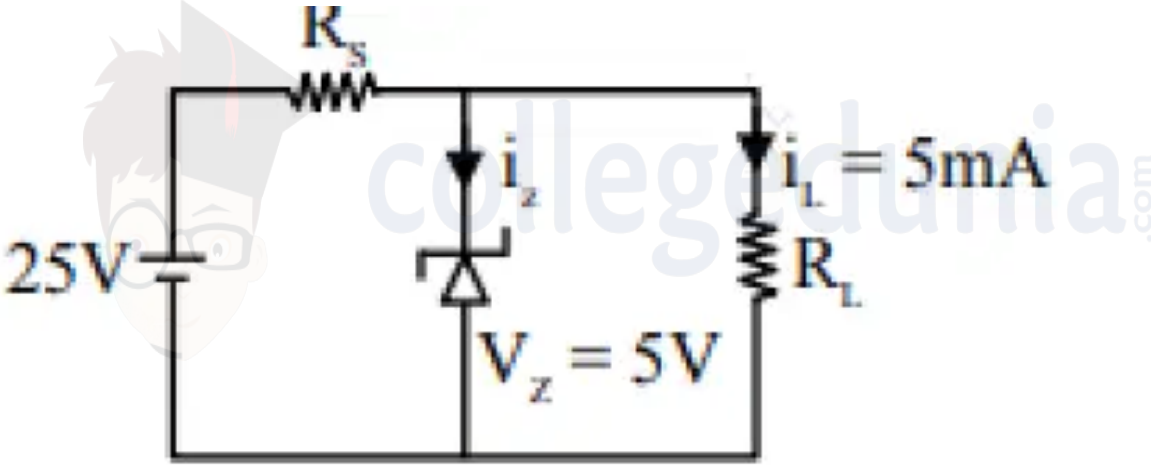
A	B	C
0	0	0
1	0	0
0	1	0
1	1	1

d.

A	B	C
0	0	0
1	0	1
0	1	0
1	1	1

---

9. In the given circuit diagram, $I_L = 5$ mA and the Zener voltage is $V_Z = 5$ V. If $i_z = 4i_L$, find the value of R_s (in Ω). **(+4, -1)**



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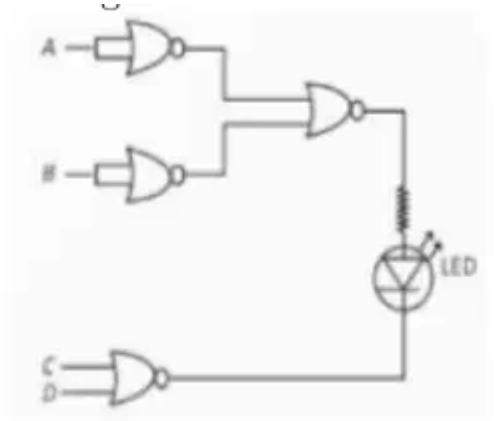
10. In the given logic circuit shown in the figure, inputs A, B, C, and D are applied as shown. An LED is connected at the output. In which of the following combinations will the LED glow? **(+4, -1)**



a. $A = 1, B = 1, C = 0, D = 0$

b. $A = 1, B = 0, C = 0, D = 0$

c. $A = 0, B = 1, C = 0, D = 0$

d. $A = 1, B = 1, C = 1, D = 1$

---

11. Given below are two statements : Statement I : PN junction diodes can be used to function as transistor, simply by connecting two diodes, back to back, which acts as the base terminal. Statement II : In the study of transistor, the amplification factor β indicates ratio of the collector current to the base current. In the light of the above statements, choose the correct answer. **(+4, -1)**

a. Both Statement I and Statement II are true

b. Both Statement I and Statement II are false

c. Statement I is true but Statement II is false

d. Statement I is false but Statement II is true

---

12. Zener breakdown occurs in a p-n junction having p and n both : **(+4, -1)**

a. lightly doped and have narrow depletion layer.

b. lightly doped and have wide depletion layer.

c. heavily doped and have narrow depletion layer.

d. heavily doped and have wide depletion layer.

---

13. An npn transistor operates as a common emitter amplifier with a power gain of 10^6. The input circuit resistance is 100 Ω and the output load resistance is 10 kΩ. The common emitter current gain 'β' will be _____. (Round off to the Nearest Integer) (+4, -1)

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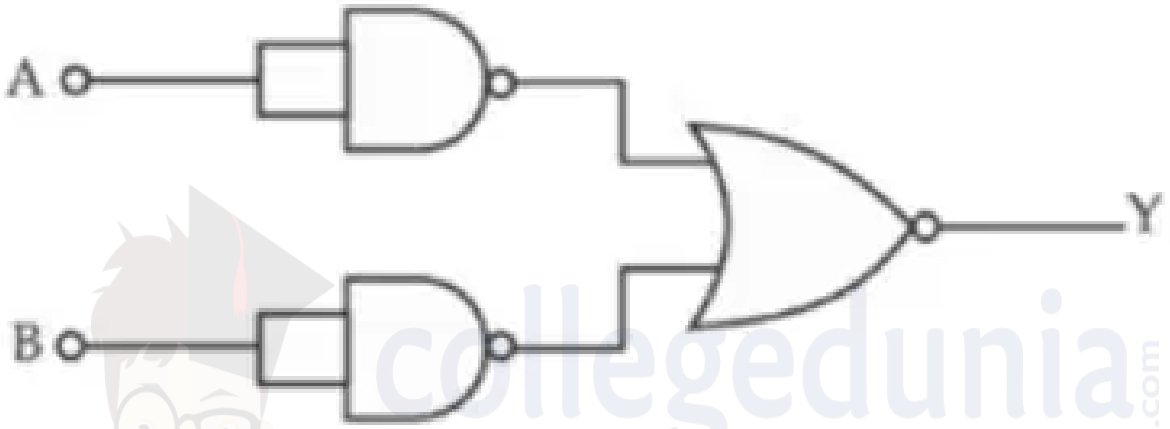
14. Identify the logic operation carried out. (+4, -1)



a. AND

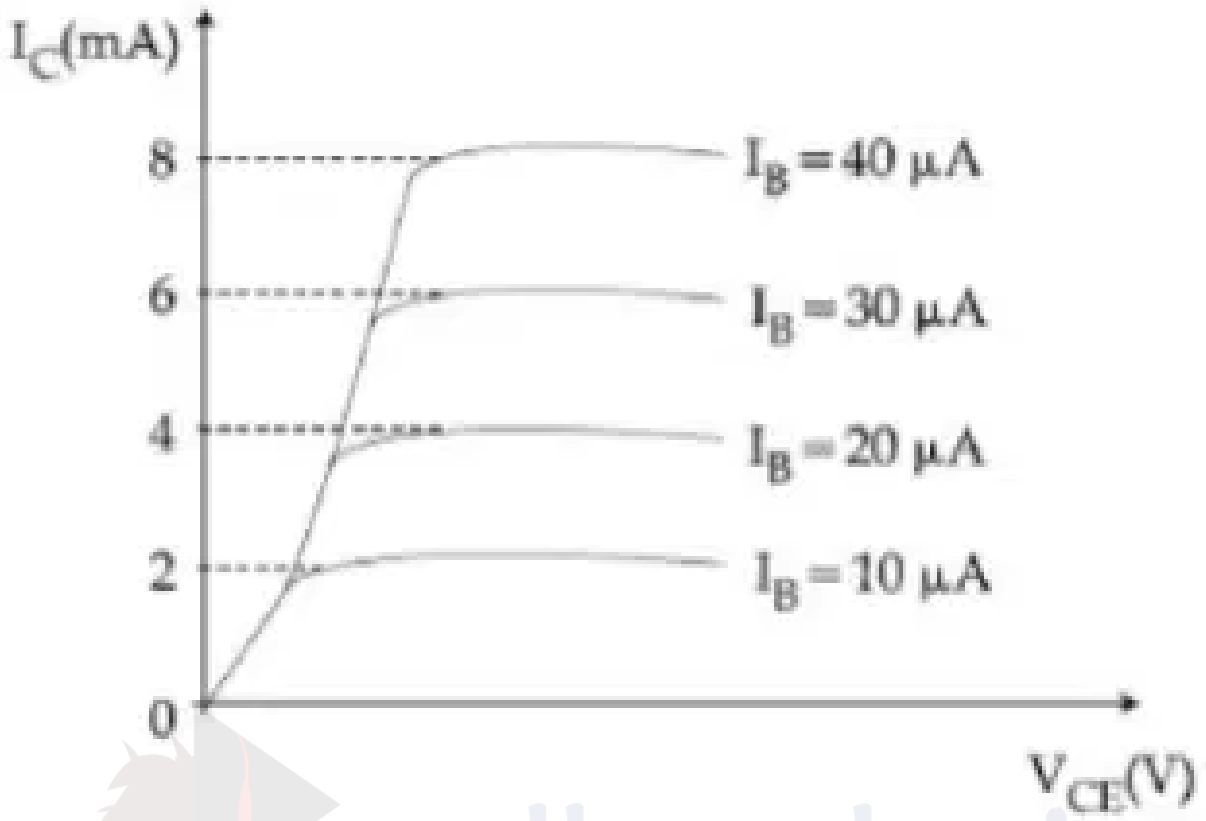
b. NAND

c. NOR

d. OR

---

15. The typical output characteristics curve for a transistor working in the common-emitter configuration is shown in the figure. The estimated current gain from the figure is _____. (+4, -1)



16. The correct relation between α (ratio of I_C to I_E) and β (ratio of I_C to I_B) of a transistor is: (+4, -1)

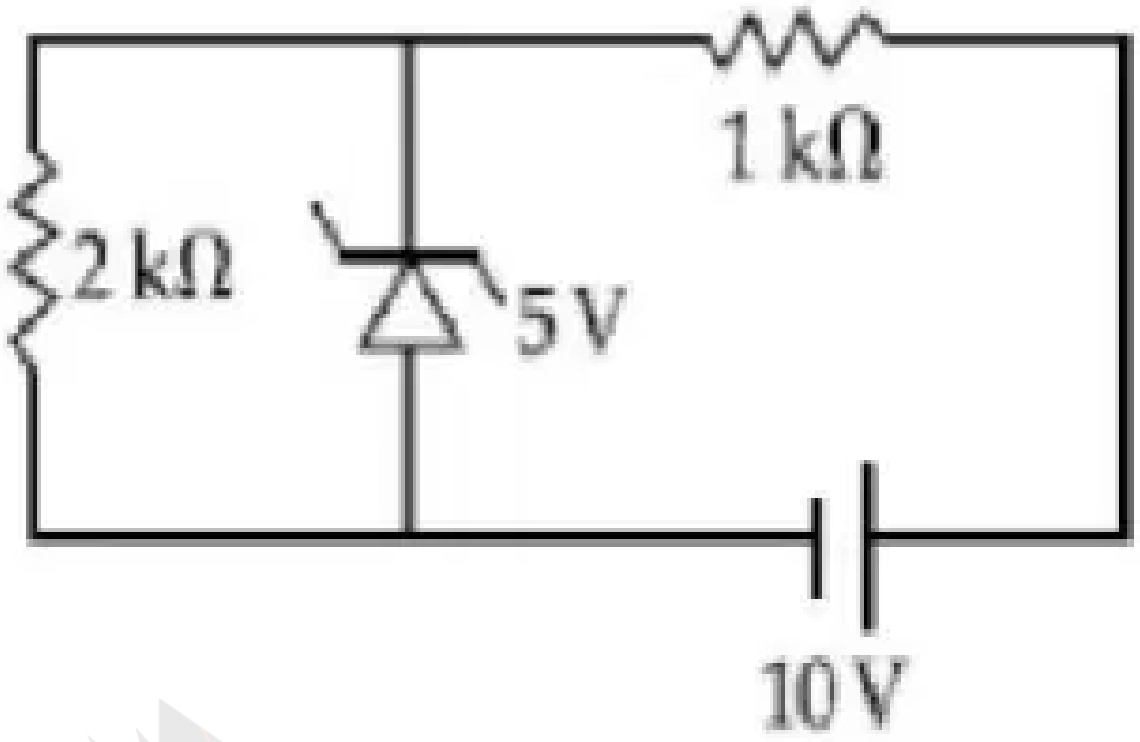
a. $\beta = \frac{\alpha}{1+\alpha}$

b. $\alpha = \frac{\beta}{1-\alpha}$

c. $\beta = \frac{1}{1-\alpha}$

d. $\alpha = \frac{\beta}{1+\beta}$

17. In connection with the circuit drawn below (assuming a Zener diode circuit with $V_z = 10V$, $R_s = 500\Omega$, $R_L = 2k\Omega$, $V_{in} = 15V$), the value of current flowing through 2 kΩ resistor is _____ × 10⁻⁴ A. (+4, -1)



18. If an emitter current is changed by 4 mA, the collector current changes by 3.5 mA. The value of β will be : (+4, -1)

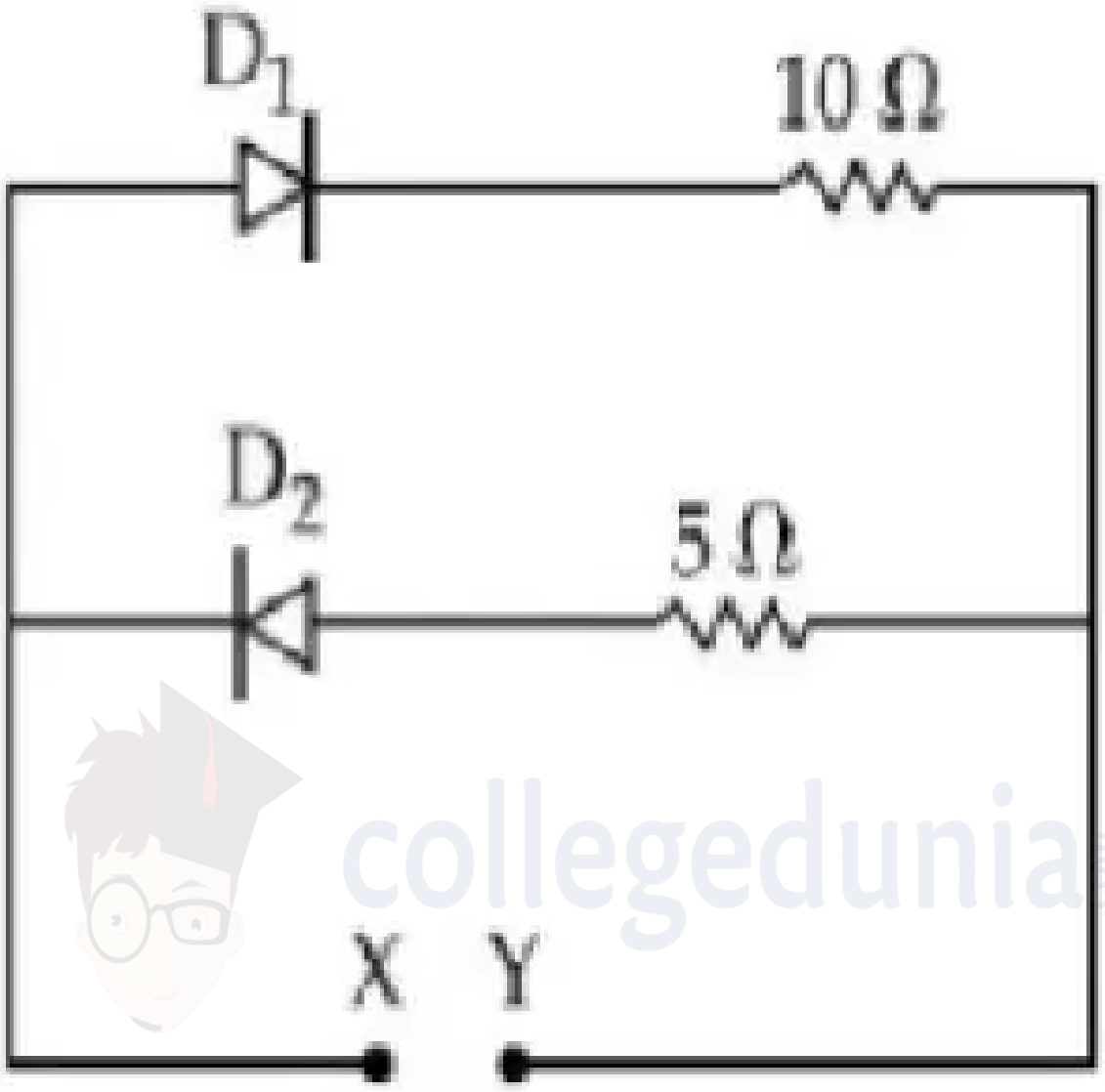
a. 7

b. 0.875

c. 0.5

d. 3.5

19. A 5V battery is connected across the points X and Y. Assume D1 and D2 to be normal silicon diodes. Find the current supplied by the battery if the +ve terminal of the battery is connected to point X and -ve to point Y. (+4, -1)



a. ~0.5 A

b. ~0.43 A

c. ~0.86 A

d. ~1.5 A

---

20. A transistor is connected in common emitter circuit configuration, the collector supply voltage is 10 V and the voltage drop across a resistor of 1000 Ω in the collector circuit is 0.6 V. If the current gain factor (β) is 24, then the base current is _____ μA. (Round off to the Nearest Integer) (+4, -1)

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21. **Match List I with List II.** **(+4, -1)**

Match List I with List II.

	List I		List II
(a)	Rectifier	(i)	Used either for stepping up or stepping down the a.c. voltage
(b)	Stabilizer	(ii)	Used to convert a.c. voltage into d.c. voltage
(c)	Transformer	(iii)	Used to remove any ripple in the rectified output voltage
(d)	Filter	(iv)	Used for constant output voltage even when the input voltage or load current change

Choose the correct answer from the options given below:

a. (a)-(ii), (b)-(i), (c)-(iii), (d)-(iv)

b. (a)-(ii), (b)-(iv), (c)-(i), (d)-(iii)

c. (a)-(ii), (b)-(i), (c)-(iv), (d)-(iii)

d. (a)-(iii), (b)-(iv), (c)-(i), (d)-(ii)

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22. **For extrinsic semiconductors; when doping level is increased;** **(+4, -1)**

a. Fermi-level of p-type semiconductor will go upward and Fermi-level of n-type semiconductors will go downward.

b. Fermi-level of p-type semiconductors will go downward and Fermi-level of n-type semiconductor will go upward.

c. Fermi-level of p and n-type semiconductors will not be affected.

d. Fermi-level of both p-type and n-type semiconductors will go upward for T>T_F K and downward for T<T_F K, where T_F is Fermi temperature.

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23. **Statement I : To get a steady dc output from the pulsating voltage received from a full wave rectifier we can connect a capacitor across the output parallel to the load R_L.**
Statement II : To get a steady dc output from the pulsating voltage received from a full wave rectifier we can connect an inductor in series with R_L. **(+4, -1)**

In the light of the above statements, choose the most appropriate answer from the options given below :

a. Both Statement I and Statement II are true

b. Both Statement I and Statement II are false

c. Statement I is true but Statement II is false

d. Statement I is false but Statement II is true

---

24. **If V_A and V_B are the input voltages (either 5 V or 0 V) and V_o is the output voltage then the two gates represented in the following circuits (A) and (B) are :** **(+4, -1)**

\begin{center} \includegraphics[width=0.5\textwidth]{logic_gates} \end{center}

a. NAND and NOR Gate

b. AND and OR Gate

c. AND and NOT Gate

d. OR and NOT Gate

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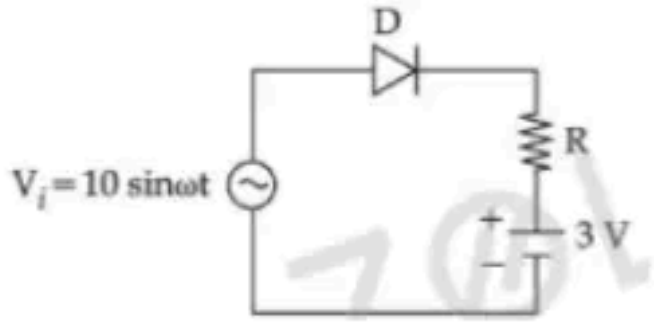
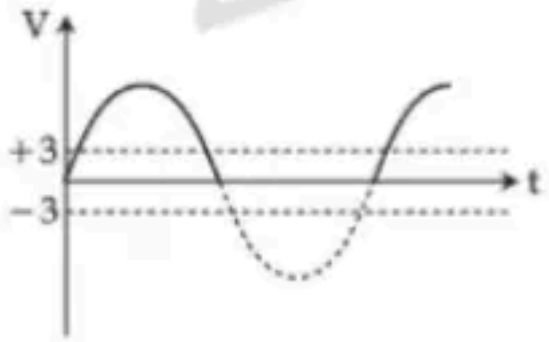
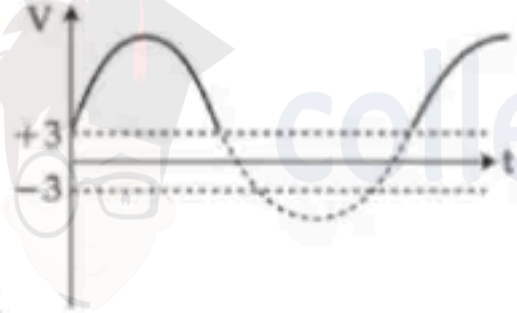
25. **Choose the correct waveform that can represent the voltage across R of the following circuit, assuming the diode is ideal one :** **(+4, -1)**



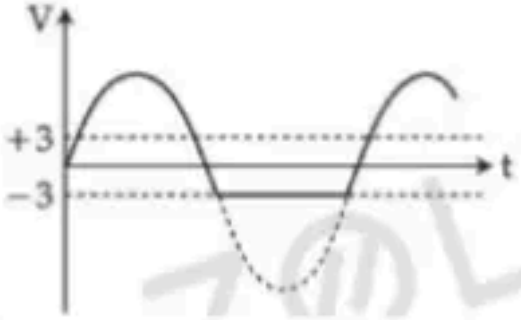
(A)



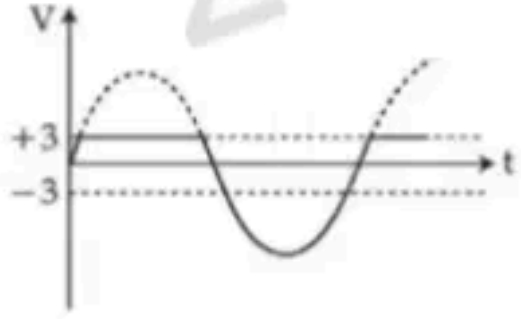
(B)



(C)



(D)



a. A

b. B

c. C

d. D

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Answers

1. **Answer: a**

Explanation:

Concept:
The given circuit is a **diode logic circuit**
with a pull-up resistor connected to $+5\ \text{V}$. Important principles:

A forward-biased diode conducts and pulls the output LOW.
A reverse-biased diode does not conduct.
A pull-up resistor forces the output HIGH when no diode conducts.

Step 1: Circuit Observation

Inputs A and B are connected to the output node through diodes.
The output y is connected to $+5\ \text{V}$ through a resistor.

Step 2: Input Condition Analysis

If **any input is LOW**
$(A = 0$ or $B = 0)$: The corresponding diode becomes forward biased and pulls the output y LOW.
If **both inputs are HIGH**
$(A = 1, B = 1)$: Both diodes are reverse biased, no current flows, and the pull-up resistor pulls y HIGH.

Step 3: Truth Table

A	B	y
0	0	0
0	1	0
1	0	0
1	1	1

Conclusion:
The output is HIGH only when both inputs are HIGH. Therefore, the circuit functions as an **AND gate**
.

---

2. Answer: d

Explanation:

Step 1: Reaction with acyl chloride.
The first step involves the reaction of CH_3NH_2 (methylamine) with phenylacetyl chloride (PhCOCl), which results in the formation of an amide:

$$CH_3NH_2 + PhCOCl \rightarrow PhCH_2NHCOPh.$$

Step 2: Reduction with $LiAlH_4$.
The second step involves the reduction of the amide with lithium aluminium hydride ($LiAlH_4$), which reduces the amide group to an amine, resulting in the formation of $PhCH_3$ (toluene). **Final Answer:**

$$\boxed{PhCH_3}.$$

---

3. Answer: 5 - 5

Explanation:

Step 1: Use Ohm's law to find the current.
Ohm's law states that the current I is related to the potential difference V, the charge density n, the charge of the carrier e, the cross-sectional area A, the length L

, and the mobility μ by the relation:

$$I = nAe\mu\frac{V}{L}.$$

Step 2: Substitute the known values.
Given: - $I = 1.2\,\text{A}$, - $A = 0.2\,\text{mm}^2 = 0.2 \times 10^{-6}\,\text{m}^2$, - $V = 2\,\text{V}$, - $L = 2\,\text{m}$, - $e = 1.6 \times 10^{-19}$, - $n = 7.5 \times 10^{28}\,\text{m}^{-3}$. Substitute these values into the equation:

$$1.2 = (7.5 \times 10^{28}) \times (0.2 \times 10^{-6}) \times (1.6 \times 10^{-19}) \times \mu \times \frac{2}{2}.$$

Simplifying this:

$$1.2 = (7.5 \times 10^{28} \times 0.2 \times 10^{-6} \times 1.6 \times 10^{-19}) \times \mu.$$

$$1.2 = (2.4 \times 10^{4}) \times \mu.$$

Step 3: Solve for μ.

$$\mu = \frac{1.2}{2.4 \times 10^{4}} = 5 \times 10^{-4}\,\text{SI units}.$$

Thus, $x = 5$. **Final Answer:**

$$\boxed{5}.$$

---

4. Answer: d

Explanation:

Step 1: Analyze Statement I.
Statement I is incorrect. The work done by a conservative force is independent of the path taken, and it depends only on the initial and final positions. The correct expression for work done by a conservative force is:

$$W = -\int_{r_1}^{r_2} f\,dr.$$

Step 2: Analyze Statement II.
Statement II is incorrect. Work done by a conservative force is path-independent, meaning it depends only on the initial and final positions, not the specific path taken.
Step 3: Conclusion.

Both statements are false. **Final Answer:**

$$\boxed{\text{Statement-I and Statement-II is false.}}.$$

---

5. Answer: c

Explanation:

Step 1: Analyze Statement 1.
The time period of a simple pendulum depends only on the length l and acceleration due to gravity g, not on the density of the material of the pendulum. Therefore, Statement 1 is false. **Step 2: Analyze Statement 2.**
The time period of a simple pendulum is indeed given by the formula:

$$T = 2\pi\sqrt{\frac{l}{g}},$$

where l is the length and g is the acceleration due to gravity. Thus, Statement 2 is true. **Step 3: Conclusion.**
Therefore, Statement I is false and Statement II is true. **Final Answer:**

$$\boxed{\text{Statement I is false; Statement II is true.}}$$

---

6. Answer: b

Explanation:

Step 1: Understanding the Concept:
In a DC circuit, a silicon diode conducts current only when it is forward-biased. Once forward-biased, it acts like a voltage source of magnitude equal to its barrier potential (0.7 V for Silicon).
Diodes that are reverse-biased act as open circuits and do not conduct current.
Step 2: Key Formula or Approach:
1. Identify biasing: Diodes A and C are forward-biased, while diode B is reverse-biased.
2. Apply Kirchhoff's Voltage Law (KVL): $V_{source} = I_{total}R + V_{diode}$.
3. Divide current: Since diodes A and C are in parallel and identical, $I_A = \frac{I_{total}}{2}$.

Step 3: Detailed Explanation:
The supply voltage is $V = 12\ \text{V}$ and the series resistance is $R = 0.3\ \text{k}\Omega = 300\Omega$.
The voltage across the parallel combination of forward-biased diodes (A and C) is fixed at the forward voltage drop: $V_f = 0.7\ \text{V}$.
The voltage drop across the resistor is:

$$V_R = V - V_f = 12 - 0.7 = 11.3\ \text{V}$$

The total current flowing out of the resistor is:

$$I_{total} = \frac{V_R}{R} = \frac{11.3\ \text{V}}{300\Omega} = \frac{11.3}{0.3}\ \text{mA} = \frac{113}{3}\ \text{mA}$$

This total current splits equally between the two parallel forward-biased diodes A and C:

$$I_A = \frac{I_{total}}{2} = \frac{113/3}{2} = \frac{113}{6}\ \text{mA}$$

Step 4: Final Answer:
The current flowing through diode A is $\frac{113}{6}$ mA.

---

7. Answer: a

Explanation:

Step 1: Understanding the Question:
A Zener diode is used as a voltage regulator. It is connected in reverse bias with a series resistor R and a DC voltage source. We are given the Zener breakdown voltage, the source voltage, and the power dissipated by the Zener diode. There is no load resistor mentioned, so all the current passing through R also passes through the Zener diode.
Step 2: Key Formula or Approach:
1. Power dissipated by Zener diode: $P_Z = V_Z \times I_Z$.
2. Current through the Zener diode: $I_Z = \frac{P_Z}{V_Z}$.
3. Since the Zener diode and the resistor R are in series, the current through the resistor I_R is equal to I_Z.
4. Voltage drop across the resistor: $V_R = V_{in} - V_Z$.

5. Using Ohm's Law, $R = \frac{V_R}{I_R}$.

Step 3: Detailed Explanation:

Given values:

Breakdown voltage of Zener, $V_Z = 10$ V

Input voltage, $V_{in} = 15$ V

Power of Zener diode, $P_Z = 0.4$ W

First, find the current flowing through the Zener diode (I_Z):

$I_Z = \frac{P_Z}{V_Z} = \frac{0.4\ \text{W}}{10\ \text{V}} = 0.04\ \text{A}$

Since there is no external load connected in parallel to the Zener, the entire current from the source flows through the series resistor R and then through the Zener diode. So, the current through the resistor is $I = I_Z = 0.04\ \text{A}$.

The voltage drop across the resistor R is the difference between the source voltage and the Zener voltage:

$V_R = V_{in} - V_Z = 15\ \text{V} - 10\ \text{V} = 5\ \text{V}$.

Now, applying Ohm's law to the resistor R:

$R = \frac{V_R}{I} = \frac{5\ \text{V}}{0.04\ \text{A}} = \frac{500}{4}\Omega = 125\Omega$.

Step 4: Final Answer:

The value of the unknown resistance R is 125 Ω.

---

8. Answer: b

Explanation:

Step 1: Understanding the Question:

We need to determine the output C for all possible binary inputs A and B for the given logic circuit and find the corresponding truth table.

Step 2: Key Formula or Approach:

We will first identify the gates and write the Boolean expression for the final output C in terms of the inputs A and B. Then, we will construct a truth table by evaluating this expression for all four possible input combinations.

Step 3: Detailed Explanation:

Let's analyze the circuit diagram.

- Gate 1: The first gate has inputs A and B. It is a D-shaped gate, which represents an AND gate. Let's call its output D. So, $D = A \cdot B$.

- Gate 2: The second gate has inputs A and D. It is a gate with a curved input side followed by a 'NOT' bubble at the output, which represents a NOR gate. Its output is C. So, $C = \overline{A + D}$.

Now, substitute the expression for D into the expression for C:

$$C = \overline{A + (A \cdot B)}$$

We can simplify this Boolean expression using absorption law: $X + X \cdot Y = X$.
Here, $A + A \cdot B = A(1 + B)$. Since $1 + B = 1$ in Boolean algebra, $A(1 + B) = A$.
So, the expression simplifies to:

$$C = \overline{A}$$

This means the output C depends only on the input A; it is the logical NOT of A.
Let's construct the truth table for $C = \overline{A}$:
- When A = 0, B = 0: $C = \overline{0} = 1$.
- When A = 0, B = 1: $C = \overline{0} = 1$.
- When A = 1, B = 0: $C = \overline{1} = 0$.
- When A = 1, B = 1: $C = \overline{1} = 0$.

The resulting truth table is:

A	B	C
0	0	1
0	1	1
1	0	0
1	1	0

Step 4: Final Answer:
The correct truth table corresponds to the output C being 1 when A is 0, and 0 when A is 1, regardless of B.

---

9. Answer: 800 - 800

Explanation:

Concept: For a Zener diode voltage regulator:
The Zener diode maintains a constant voltage V_Z across the load
Source current splits as: $I_s = I_L + I_Z$
Ohm's law is applied across the series resistance R_s
Step 1: Given data Load current:

$$I_L = 5\ \text{mA}$$

Given:

$$i_z = 4i_L \Rightarrow I_Z = 4 \times 5 = 20 \text{ mA}$$

Step 2: Calculate source current

$$I_s = I_L + I_Z = 5 + 20 = 25 \text{ mA}$$

Step 3: Voltage across series resistance Supply voltage:

$$V_s = 25 \text{ V}$$

Zener voltage:

$$V_Z = 5 \text{ V}$$

$$V_{R_s} = V_s - V_Z = 25 - 5 = 20 \text{ V}$$

Step 4: Find R_s using Ohm's law

$$R_s = \frac{V_{R_s}}{I_s} = \frac{20}{25 \times 10^{-3}} = 800 \ \Omega$$

Step 5: Hence,

$$\boxed{R_s = 800 \ \Omega}$$

---

10. Answer: d

Explanation:

Step 1: Analyze the logic gates.
In the given logic circuit, A and B are inputs to an AND gate, and the output of this AND gate is input to another gate along with C and D. The LED will glow when the output of the logic circuit is high (i.e., when the combined output of the gates is 1).
Step 2: Apply the logic gate operation.
After applying the truth table for the AND and OR gates in the circuit, we find that the LED will glow when $A = 1$, $B = 1$, $C = 1$, and $D = 1$. **Step 3: Conclusion.**

Thus, the LED will glow in option (4). **Final Answer:**

$$\boxed{A = 1, B = 1, C = 1, D = 1}$$

---

11. Answer: d

Explanation:

Step 1: Statement I is **false**. A transistor is a single crystal with three regions. Back-to-back diodes have two separate depletion layers and no interaction between the "emitter" and "collector" through a shared thin base.
Step 2: Statement II is **true**. β (Current gain in CE mode) $= I_C/I_B$.

---

12. Answer: c

Explanation:

Step 1: Zener breakdown occurs due to high electric field intensity across the junction.
Step 2: **Heavy doping** increases the concentration of charge carriers, which results in a very **narrow depletion layer**.
Step 3: A narrow layer creates a massive electric field $(E = V/d)$ even at low voltages, enabling electrons to tunnel through.

---

13. Answer: 100 - 100

Explanation:

Step 1: Power Gain (P_{gain}) = (Current Gain)^2 $\times$ Resistance Gain. $P_{gain} = \beta^2 \times \frac{R_{out}}{R_{in}}$.
Step 2: Substitute the values: $10^6 = \beta^2 \times \frac{10{,}000}{100} = \beta^2 \times 100$.
Step 3: $\beta^2 = \frac{10^6}{100} = 10^4 \implies \beta = \sqrt{10^4} = 100$.

---

14. Answer: a

Explanation:

Step 1: Understanding the Concept:
A NAND gate with its inputs tied together acts as a NOT gate.
A NOR gate with inputs X and Y produces the output $\overline{X+Y}$.
Step 2: Key Formula or Approach:
Use Boolean algebra and De Morgan's Laws:
1. $\text{NAND}(A, A) = \bar{A}$.
2. $\text{NOR}(X, Y) = \overline{X+Y}$.
3. $\overline{\bar{A}+\bar{B}} = A \cdot B$.
Step 3: Detailed Explanation:
Input A passes through a NAND gate with shorted inputs. The output is $X = \bar{A}$.
Input B passes through a NAND gate with shorted inputs. The output is $Y = \bar{B}$.
Both X and Y are then fed into a NOR gate.
The final output Y_{out} is:

$$Y_{\text{out}} = \overline{X+Y} = \overline{\bar{A}+\bar{B}}$$

Applying De Morgan's Law ($\overline{P+Q} = \bar{P} \cdot \bar{Q}$):

$$Y_{\text{out}} = \overline{(\bar{A})} \cdot \overline{(\bar{B})} = A \cdot B$$

The logical expression $A \cdot B$ corresponds to the AND operation.
Step 4: Final Answer:
The logic operation is AND.

---

15. Answer: 200 - 200

Explanation:

Step 1: Current gain (β) in common-emitter configuration is the ratio of change in collector current (ΔI_C) to change in base current (ΔI_B) at a constant collector-emitter voltage (V_{CE}).
Step 2: From the typical graph: If I_B changes from $10\mu A$ to $20\mu A$ ($\Delta I_B = 10\mu A$), and I_C changes from $2mA$ to $4mA$ ($\Delta I_C = 2mA$).
Step 3: Calculate β.

$$\beta = \frac{\Delta I_C}{\Delta I_B} = \frac{2 \times 10^{-3}}{10 \times 10^{-6}} = 200$$

---

16. Answer: d

Explanation:

Step 1: Use the fundamental transistor current equation: $I_E = I_B + I_C$.
Step 2: Divide the entire equation by I_C:

$$\frac{I_E}{I_C} = \frac{I_B}{I_C} + \frac{I_C}{I_C} \implies \frac{1}{\alpha} = \frac{1}{\beta} + 1$$

Step 3: Solve for α:

$$\frac{1}{\alpha} = \frac{1+\beta}{\beta} \implies \alpha = \frac{\beta}{1+\beta}$$

---

17. Answer: 25 - 25

Explanation:

Step 1: In a Zener voltage regulator, the voltage across the load R_L is the Zener voltage V_z, provided V_{in} is sufficient.
Step 2: $V_L = V_z = 10$ V.
Step 3: Current through load $I_L = \frac{V_L}{R_L} = \frac{10}{2000} = 0.005$ A.
Step 4: 0.005 A $= 50 \times 10^{-4}$ A.

---

18. Answer: a

Explanation:

Step 1: Given $\Delta I_E = 4$ mA and $\Delta I_C = 3.5$ mA.
Step 2: Current gain $\alpha = \frac{\Delta I_C}{\Delta I_E} = \frac{3.5}{4} = 0.875$.
Step 3: Relation: $\beta = \frac{\alpha}{1-\alpha} = \frac{0.875}{1-0.875} = \frac{0.875}{0.125}$.
Step 4: $\beta = 7$.

---

19. Answer: b

Explanation:

Step 1: In forward bias, a silicon diode has a potential drop of 0.7 V.
Step 2: With X connected to positive and Y to negative, the diode path is forward-biased.
Step 3: Effective voltage $V_{eff} = 5 - 0.7 = 4.3$ V.
Step 4: Assuming a standard circuit resistance of $10\,\Omega$, current $I = 4.3/10 = 0.43$ A.

---

20. Answer: 25 - 25

Explanation:

First, we find the collector current (I_C) using Ohm's law for the collector resistor (R_C).
Voltage drop across R_C, $V_{R_C} = 0.6$ V.
Resistance of $R_C = 1000\,\Omega$.
$I_C = \frac{V_{R_C}}{R_C} = \frac{0.6\text{ V}}{1000\,\Omega} = 0.6 \times 10^{-3}$ A.
$I_C = 0.6$ mA.
Next, we use the current gain factor (β) to find the base current (I_B). The formula for β in a common emitter configuration is:
$\beta = \frac{I_C}{I_B}$
We are given $\beta = 24$.
Rearranging the formula to solve for I_B:
$I_B = \frac{I_C}{\beta} = \frac{0.6 \times 10^{-3}\text{ A}}{24}$
$I_B = \frac{6 \times 10^{-4}}{24} = \frac{1}{4} \times 10^{-4}\text{ A} = 0.25 \times 10^{-4}$ A.
The question asks for the answer in microamperes (μA).
$1\,\mu\text{A} = 10^{-6}$ A.
$I_B = 0.25 \times 10^{-4}\text{ A} = 25 \times 10^{-6}\text{ A} = 25\,\mu\text{A}$.
The nearest integer is 25.

---

21. Answer: b

Explanation:

Let's match each component from List I with its function from List II.
(a) Rectifier: A device that converts alternating current (AC) to direct current (DC).
This matches with (ii) "Used to convert a.c. voltage into d.c. voltage".

(b) Stabilizer: A device designed to maintain a constant output voltage, regardless of fluctuations in the input voltage or load. This matches with (iv) "Used for constant output voltage...".
(c) Transformer: A device that transfers electrical energy from one AC circuit to another, either increasing (stepping up) or decreasing (stepping down) the voltage. This matches with (i) "Used either for stepping up or stepping down the a.c. voltage".
(d) Filter: In the context of a power supply, a filter is used to smooth the pulsating DC output from a rectifier, removing the unwanted AC components known as ripples. This matches with (iii) "Used to remove any ripple in the rectified output voltage".
The correct matching is: (a)-(ii), (b)-(iv), (c)-(i), (d)-(iii). This corresponds to option (B).

---

22. Answer: b

Explanation:

Let's consider the effect of doping on the Fermi level for both n-type and p-type semiconductors.
In an intrinsic semiconductor, the Fermi level (E_F) is located near the middle of the band gap between the valence band (E_V) and the conduction band (E_C).
For an n-type semiconductor, donor impurities are added. These donors create energy levels just below the conduction band. Increasing the doping level increases the concentration of donor atoms and thus the concentration of free electrons in the conduction band. This higher electron concentration shifts the Fermi level upwards, closer to the conduction band.
For a p-type semiconductor, acceptor impurities are added. These acceptors create energy levels just above the valence band. Increasing the doping level increases the concentration of acceptor atoms and thus the concentration of holes in the valence band. This higher hole concentration shifts the Fermi level downwards, closer to the valence band.
Therefore, when the doping level is increased, the Fermi-level of a p-type semiconductor will go downward, and the Fermi-level of an n-type semiconductor will go upward.

---

23. Answer: a

Explanation:

Step 1: Understanding the Concept:
A rectifier converts AC to pulsating DC. To smooth these pulsations (ripples) and obtain a steady DC voltage, filter circuits using capacitors or inductors are used.
Step 2: Detailed Explanation:
Statement I: A capacitor filter works by charging during the peak of the pulsating voltage and discharging through the load when the voltage drops. Since it stores charge, it maintains a higher voltage level across the load, reducing ripples. It must be connected in **parallel** with the load. So Statement I is true.
Statement II: An inductor has the property of opposing any change in current. When placed in **series** with the load, it smooths out the variations in the current flow, effectively filtering the AC components out of the pulsating DC. So Statement II is true.
Step 3: Final Answer:
Both methods are valid techniques for filtering rectified voltage. Thus, both statements are true.

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24. **Answer: d**

Explanation:

Step 1: Understanding the Concept:
Logic gates can be constructed using electronic components like diodes and transistors. Diodes act as switches for specific voltage levels, while transistors can invert signals in a common-emitter configuration.
Step 2: Detailed Explanation:
Circuit (A): This circuit uses two diodes in parallel connected to a resistor leading to ground. - If $V_A = 5V$ or $V_B = 5V$, the corresponding diode becomes forward biased, allowing current to flow. The output V_o becomes high ($\approx 5V$). - The output is low ($0V$) only when both inputs are low. This is the logic for an **OR gate**.
Circuit (B): This is a standard NPN transistor inverter circuit. - If $V_B = 5V$ (High), the transistor is switched ON (saturated), effectively connecting the output V_o to ground. Thus, $V_o = 0V$ (Low). - If $V_B = 0V$ (Low), the transistor is switched OFF, and V_o is pulled up to 5V through the collector resistor R_C. - This inversion of logic defines a **NOT gate**.

Step 3: Final Answer:
Circuit (A) is an OR gate and Circuit (B) is a NOT gate.

---

25. Answer: a

Explanation:

Step 1: Understanding the Concept:
The circuit contains an AC source $V_i = 10 \sin \omega t$, an ideal diode D, a resistor R, and a 3V DC battery.
The diode is ideal, acting as a short circuit when forward-biased and an open circuit when reverse-biased.
The diode will conduct only when the potential at its anode is greater than the potential at its cathode.
Step 2: Key Formula or Approach:
Using Kirchhoff's Voltage Law (KVL), the condition for the diode to conduct is:

$$V_i > 3\text{V}$$

When the diode conducts ($V_i > 3\text{V}$), the voltage across the resistor V_R is:

$$V_R = V_i - 3$$

When the diode does not conduct ($V_i \leq 3\text{V}$), the current in the circuit is zero:

$$V_R = 0$$

Step 3: Detailed Explanation:
1. During the positive half cycle, the input voltage V_i increases from 0V to 10V.
2. As long as $V_i < 3\text{V}$, the diode is reverse-biased, and $V_R = 0$.
3. Once V_i exceeds 3V, the diode becomes forward-biased (ON).
4. The voltage V_R follows the shape of the input wave but is shifted down by 3V.
5. The peak value of V_R will be $10\text{V} - 3\text{V} = 7\text{V}$.
6. During the negative half cycle, V_i is negative, making the anode lower than the cathode, so the diode remains OFF and $V_R = 0$.
Step 4: Final Answer:
The resulting waveform should be zero until the input reaches 3V, then rise to a

peak and return to zero when the input falls below 3V.
This matches the waveform shown in option (A).

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