The Collegedunia NCERT Notes

The Ultimate NCERT Guide for Class 12 Physics

Chapter 14: Semiconductor Electronics

1 Classification of Metals, Conductors, and Semiconductors

1.1 Introduction

The electrical conductivity of solids is one of the most important physical properties that distinguishes materials. Based on their resistivity (ρ) or conductivity ($\sigma = 1/\rho$), solids can be broadly classified into three categories.

Classification Based on Resistivity

1. **Metals (Conductors):**
   - Resistivity: $\rho \sim 10^{-2}$ to $10^{-8}\,\Omega$m.
   - Conductivity: $\sigma \sim 10^{2}$ to 10^{8} S/m.
   - Examples: Copper, Aluminium, Silver.
2. **Semiconductors:**
   - Resistivity: $\rho \sim 10^{-5}$ to $10^{6}\,\Omega$m.
   - Conductivity: $\sigma \sim 10^{5}$ to 10^{-6} S/m.
   - Examples: Silicon (Si), Germanium (Ge), Gallium Arsenide (GaAs).
3. **Insulators:**
   - Resistivity: $\rho \sim 10^{11}$ to $10^{19}\,\Omega$m.
   - Conductivity: $\sigma \sim 10^{-11}$ to 10^{-19} S/m.
   - Examples: Glass, Rubber, Diamond.

1.2 Energy Bands in Solids

The behaviour of electrons in a solid is best explained using the Band Theory of Solids. When a large number of atoms are brought together to form a solid, the discrete energy levels of isolated atoms split and form closely spaced energy bands due to interatomic interactions.

Formation of Energy Bands

- In an isolated atom, electrons occupy discrete energy levels (e.g., 1s, 2s, 2p).
- As two atoms approach each other, each energy level splits into two closely spaced levels due to wavefunction overlap (Pauli's exclusion principle).
- When N atoms combine to form a solid, each energy level splits into N extremely close energy levels, effectively forming a continuous **energy band**.
- The splitting is most pronounced for the outermost (valence) electrons, as their wavefunctions overlap first. Inner electron levels are less affected.

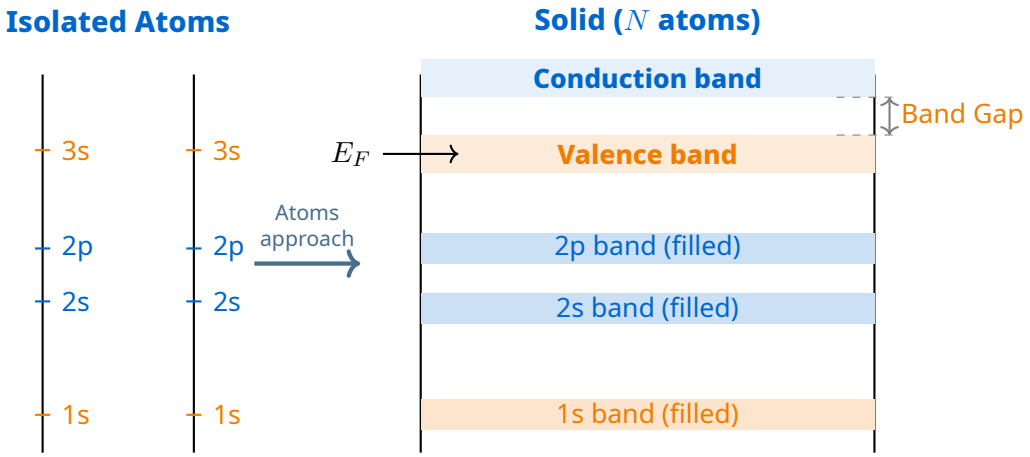


Figure 1: When atoms form a solid, discrete atomic energy levels split into nearly continuous energy bands. The highest filled band is the valence band, and the next empty band is the conduction band.

1.3 Key Terminology in Band Theory

Before we classify materials, we must define the crucial energy bands and the gap between them.

Valence Band, Conduction Band, and Band Gap

- **Valence Band (VB):** The highest energy band that is completely filled with electrons at 0 K. Electrons in this band are bound to the atom and cannot contribute to electrical conduction.
- **Conduction Band (CB):** The lowest energy band that is completely empty at 0 K. If electrons are excited into this band, they are free to move and conduct electricity.

- **Forbidden Energy Gap (E_g):** The energy range between the top of the valence band and the bottom of the conduction band. No electron states can exist here. It is the minimum energy required to raise an electron from the VB to the CB.
- **Fermi Level (E_F):** The highest occupied energy level in a material at absolute zero (0 K). Its position relative to the bands determines the material's properties.

1.4 Classification Based on Band Structure

The difference between conductors, insulators, and semiconductors lies in their energy band structures.

Band Structure of Different Materials

1. Conductors (e.g., Copper): The conduction band and valence band **overlap** each other, or the conduction band is partially filled. Therefore, there is no energy gap. Even at 0 K, electrons can move easily, resulting in very high conductivity. A small applied electric field can accelerate these electrons.

- $E_g = 0$ eV.
- E_F lies inside an allowed band.

2. Insulators (e.g., Diamond): The valence band is completely filled, the conduction band is completely empty, and the forbidden energy gap (E_g) is very large (> 3 eV). Thermal energy at room temperature ($k_BT \approx 0.025$ eV) is far too small to excite electrons from VB to CB. Therefore, no current can flow.

- $E_g > 3$ eV (Diamond: 5.5 eV).
- E_F lies in the middle of the band gap.

3. Semiconductors (e.g., Silicon): They have a band structure similar to insulators, but the forbidden energy gap (E_g) is small (typically < 3 eV). At 0 K, they behave as perfect insulators. At room temperature, some electrons gain enough thermal energy to jump from the VB to the CB. This creates a small but measurable conductivity.

- $E_g \approx 0.2$ eV to 3 eV (Si: 1.1 eV, Ge: 0.7 eV).
- E_F lies roughly in the middle of the band gap.

Key Points to Remember

- **Conductivity** depends on the number of free charge carriers (electrons in CB and holes in VB).

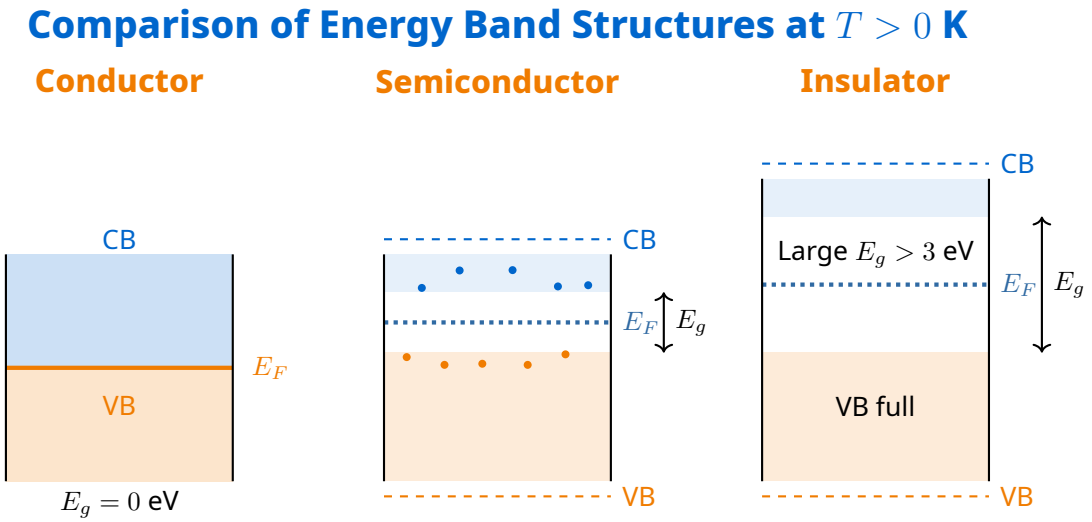


Figure 2: Schematic representation of energy bands in conductors, semiconductors, and insulators. The Fermi level (E_F) is indicated by the dotted line.

- **Semiconductors at 0 K** are perfect insulators. Their conductivity increases with temperature, unlike conductors.
- **Typical E_g values:** Carbon (diamond): 5.5 eV (Insulator), Silicon (Si): 1.1 eV, Germanium (Ge): 0.72 eV (Semiconductors).

2 Intrinsic and Extrinsic Semiconductors

2.1 Intrinsic Semiconductor

An intrinsic (or pure) semiconductor is a semiconductor in its purest form, without any significant dopant atoms. The most common examples are pure Silicon (Si) and Germanium (Ge).

Intrinsic Semiconductor

A semiconductor in which the number of electrons in the conduction band is **exactly equal** to the number of holes in the valence band at any given temperature is called an intrinsic semiconductor.

$$n_i = p_i = n_i$$

Where n_i is the intrinsic carrier concentration.

- At $T = 0$ K, it behaves like a perfect insulator ($n_i = p_i = 0$).
- At room temperature ($T \approx 300$ K), some covalent bonds break due to thermal energy, generating electron-hole pairs (EHPs).

2.2 Mechanism of Conduction in Intrinsic Semiconductors

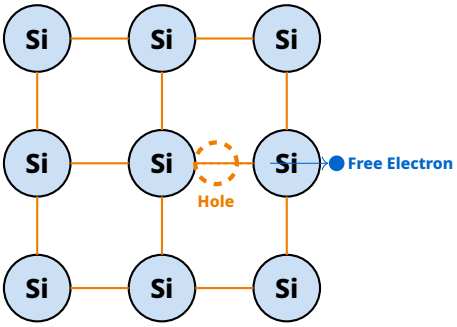
In a silicon crystal, each atom shares its four valence electrons with four neighbouring atoms, forming covalent bonds. At room temperature, thermal vibrations can break these bonds.

Electron-Hole Pair (EHP) Generation

- When a covalent bond breaks, the electron that was part of the bond becomes free to move throughout the crystal. It enters the **conduction band**.
- The empty space left behind in the bond is called a **hole**. A hole behaves as a positive charge carrier with a magnitude of charge equal to that of an electron ($+e$).
- **Recombination:** An electron from the CB can meet a hole in the VB, releasing energy (often as heat or light).
- At thermal equilibrium, the rate of generation of EHPs equals the rate of recombination.

Bond Breaking: Bond $\xrightarrow{\text{Thermal Energy}}$ Free Electron (e^-) + Hole (h^+)

Intrinsic Silicon Crystal (2D Representation)



A broken covalent bond creates a free electron and a hole.

Figure 3: A 2D schematic of the silicon lattice. A thermally broken bond generates a pair of charge carriers: a free electron in the conduction band and a hole in the valence band.

2.3 Extrinsic Semiconductor

The conductivity of an intrinsic semiconductor is very low for practical applications. To increase conductivity, a controlled amount of suitable impurity atoms (dopants) is added. This process is called **doping**.

Extrinsic Semiconductor

A semiconductor whose conductivity has been significantly increased by the addition of a small percentage of foreign atoms (impurities) is called an extrinsic semiconductor.

- **Doping:** The deliberate process of adding a trivalent (3 valence electrons) or pentavalent (5 valence electrons) impurity to a pure semiconductor.
- **Doping concentration:** Typically very small, about 1 atom in 10^6 to 10^8 semiconductor atoms.
- Extrinsic semiconductors are primarily of two types: **n-type** and **p-type**.

2.4 n-type Semiconductor

An n-type semiconductor is formed by doping an intrinsic semiconductor with a **pentavalent** impurity atom (e.g., Phosphorus P, Arsenic As, Antimony Sb). These are called **donor impurities**.

Formation of n-type Semiconductor

1. The pentavalent impurity atom replaces a silicon atom in the lattice.
2. Four of its five valence electrons form covalent bonds with the four neighbouring silicon atoms.
3. The **fifth electron** is very loosely bound to the parent impurity atom (binding energy ≈ 0.01 eV for Ge, ≈ 0.05 eV for Si).
4. At room temperature, this extra electron is easily detached and enters the conduction band, becoming a free charge carrier.
5. The impurity atom becomes a positively charged, immobile ion (e.g., P^+).

Majority & Minority Carriers:

- **Majority Carriers:** Electrons ($n_n \gg n_i$).
- **Minority Carriers:** Holes ($p_n \ll n_i$). The subscript 'n' denotes an n-type material.
- The crystal remains electrically neutral ($n_n = N_D + p_n \approx N_D$, where N_D is the donor concentration).

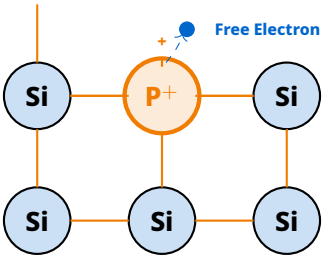


Figure 4: 2D schematic of an n-type semiconductor. The pentavalent dopant (e.g., Phosphorus) provides an extra electron that is free to move, increasing the electron concentration.

2.5 p-type Semiconductor

A p-type semiconductor is formed by doping an intrinsic semiconductor with a **trivalent** impurity atom (e.g., Boron B, Aluminium Al, Gallium Ga). These are called **acceptor impurities**.

Formation of p-type Semiconductor

1. The trivalent impurity atom replaces a silicon atom in the lattice.
2. It has only three valence electrons, so it forms covalent bonds with three of its four neighbouring silicon atoms.
3. A vacancy is created in the fourth bond, which acts as a **hole**.
4. This hole can easily accept an electron from a nearby silicon bond (ionization energy ≈ 0.01 eV).
5. The impurity atom becomes a negatively charged, immobile ion (e.g., B^-).

Majority & Minority Carriers:

- **Majority Carriers:** Holes ($p_p \gg n_i$).
- **Minority Carriers:** Electrons ($n_p \ll n_i$). The subscript 'p' denotes a p-type material.
- The crystal remains electrically neutral ($p_p = N_A + n_p \approx N_A$, where N_A is the acceptor concentration).

2.6 Energy Band Diagram of Extrinsic Semiconductors

Doping not only changes carrier concentrations but also shifts the Fermi level and introduces donor/acceptor energy levels within the band gap.

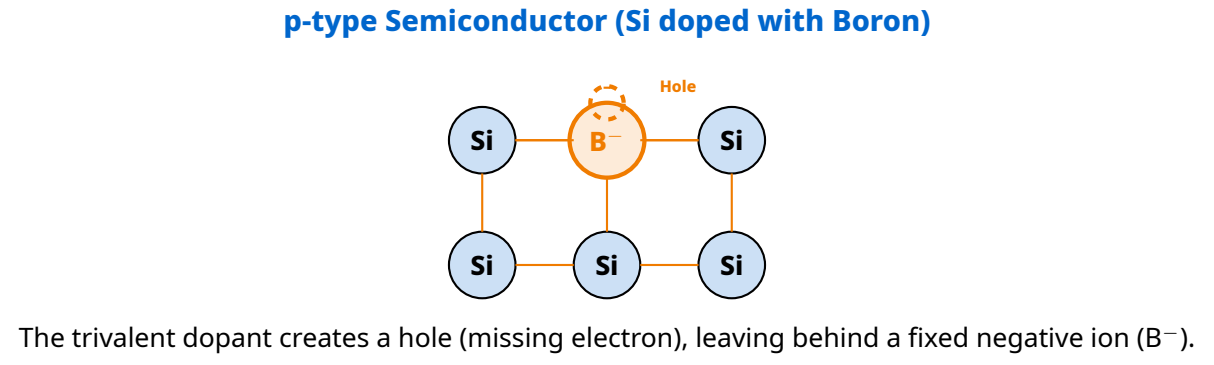


Figure 5: 2D schematic of a p-type semiconductor. The trivalent dopant (e.g., Boron) is unable to complete four covalent bonds, creating a hole that is available for conduction.

Donor and Acceptor Energy Levels

- **Donor Level (E_D):** In n-type semiconductors, the energy level of the extra, loosely bound electron lies just **below the conduction band** (distance $\approx 0.01 - 0.05$ eV). At room temperature, these electrons are easily excited into the CB. The Fermi level (E_F) shifts upward, closer to the CB.
- **Acceptor Level (E_A):** In p-type semiconductors, the energy level of the hole lies just **above the valence band** (distance $\approx 0.01 - 0.05$ eV). Electrons from the VB can easily jump into these levels, leaving holes in the VB. The Fermi level (E_F) shifts downward, closer to the VB.

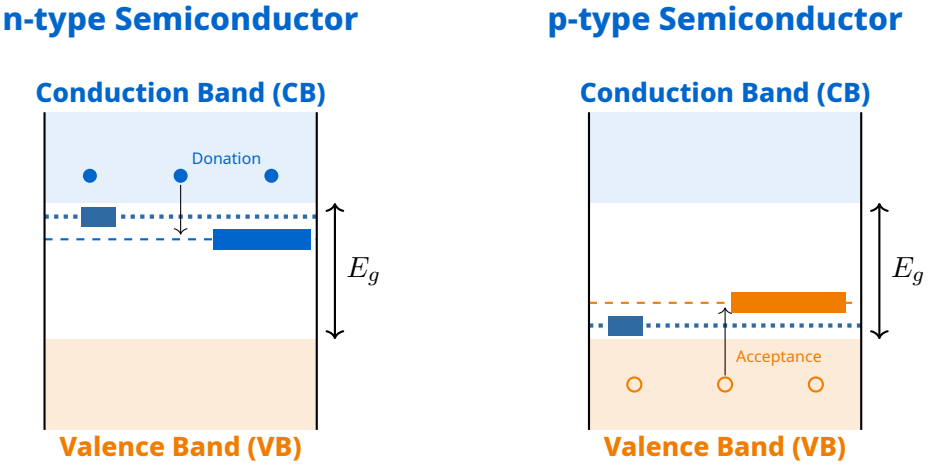


Figure 6: Optimized internal labeling for n-type and p-type semiconductors.

Important Formulas and Concepts

Law of Mass Action (at thermal equilibrium): In any semiconductor, intrinsic or extrinsic, the product of electron and hole concentrations is a constant at a given temperature, equal to the square of the intrinsic concentra-

tion.

$$\boxed{n \times p = n_i^2}$$

Electrical Neutrality Condition: An extrinsic semiconductor as a whole is electrically neutral.

For n-type: $n_n = N_D + p_n \approx N_D$
For p-type: $p_p = N_A + n_p \approx N_A$

Conductivity (σ):

$$\sigma = e(n\mu_e + p\mu_h)$$

Where μ_e and μ_h are the mobilities of electrons and holes, respectively.

3 The p-n Junction

3.1 What is a p-n Junction?

A p-n junction is the fundamental building block of most semiconductor devices. It is not formed by merely placing a p-type crystal next to an n-type crystal. It is a single crystal that is appropriately doped in two adjacent regions.

p-n Junction

A **p-n junction** is a boundary or interface formed within a single crystal of a semiconductor when one side is doped with acceptor impurities (p-type) and the other side with donor impurities (n-type).

- It is the fundamental unit of semiconductor diodes, transistors, solar cells, LEDs, and integrated circuits.
- The region where the doping transitions from p-type to n-type is called the **metallurgical junction**.
- Fabrication methods: Alloying, Diffusion, Ion Implantation, and Epitaxial Growth.

3.2 Formation of the Depletion Region

The moment a p-n junction is formed, a very important process occurs due to the large concentration gradients of charge carriers across the junction.

Diffusion and Drift at the Junction

1. Diffusion Current:

- Holes from the p-region (where they are majority carriers) diffuse into the n-region.

- Electrons from the n-region (where they are majority carriers) diffuse into the p-region.
- This is a natural process driven by the concentration gradient.

2. Formation of Ions (Space Charge Region):

- When a hole moves from the p-side to the n-side, it leaves behind an immobile, negatively charged acceptor ion (e.g., B^-).
- When an electron leaves the n-side, it leaves behind an immobile, positively charged donor ion (e.g., P^+).
- Near the junction, a region depleted of any mobile charge carriers is created. This is called the **depletion region** (or space charge region).

3. Built-in Potential (V_{bi}) / Barrier Potential:

- The immobile ions create an internal electric field directed from the positive ions (n-side) to the negative ions (p-side).
- This field opposes further diffusion. An equilibrium is reached when the drift current (due to this field) exactly balances the diffusion current.
- The potential difference associated with this field is the **barrier potential**, V_{bi}.
- $V_{bi} \approx 0.3$ V for Ge and 0.7 V for Si.

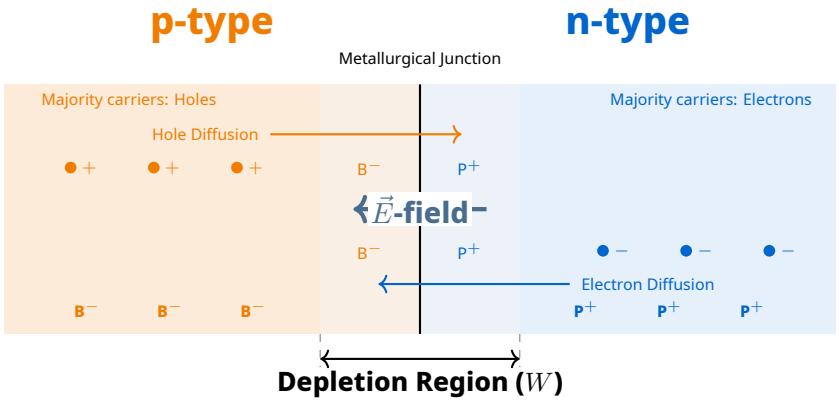


Figure 7: Formation of the depletion region in a p-n junction.

3.3 Energy Band Diagram of a p-n Junction

The internal electric field in the depletion region causes a bending of the energy bands. This brilliantly depicts the barrier that carriers must overcome.

Band Bending at Equilibrium

- Before joining, the Fermi level (E_F) in p-type is near VB, and E_F in n-type is near CB.
- At thermal equilibrium, the Fermi level must be constant throughout the entire system. This fundamental principle forces the energy bands (CB and VB) to bend by an amount equal to the contact potential qV_{bi}.
- The amount of band bending is $E_{\text{bend}} = qV_{bi}$, where q is the electron charge.
- This bending creates a potential barrier that prevents further diffusion. An electron in the n-region must gain energy qV_{bi} to cross to the p-region.

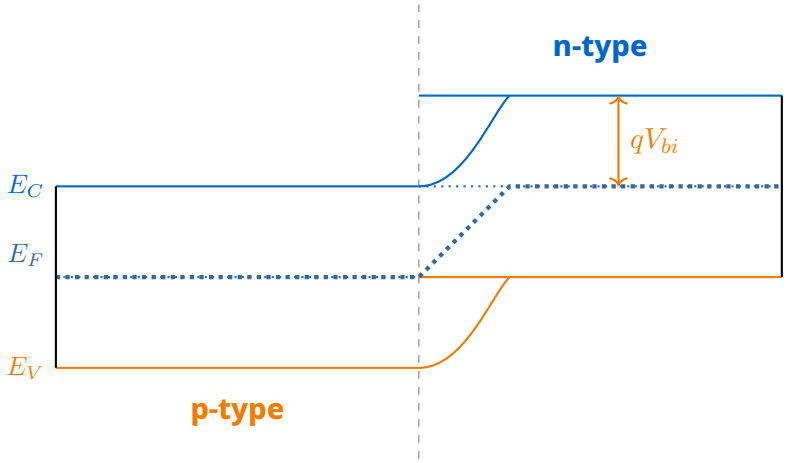


Figure 8: Energy band diagram of a p-n junction at thermal equilibrium. The Fermi level E_F is constant, forcing the bands to bend by an amount equal to qV_{bi} in the depletion region.

3.4 Biasing of a p-n Junction

Applying an external voltage to a p-n junction is called biasing. There are two fundamental modes.

3.4.1 Forward Bias

In forward bias, the p-side is connected to the positive terminal of a battery and the n-side to the negative terminal.

Forward Biased p-n Junction

Effect:

- The applied voltage opposes the internal barrier potential V_{bi}.

- The effective barrier height reduces to $q(V_{bi} - V)$, where V is the applied forward voltage.
- The depletion region width **decreases**.
- A large number of majority carriers can now diffuse across the junction, leading to a significant **forward current**.

Condition for Conduction:

$$I \text{ is appreciable if } V > V_{bi} \text{ (knee voltage)}$$

Knee voltage for Si ≈ 0.7 V, for Ge ≈ 0.3 V.

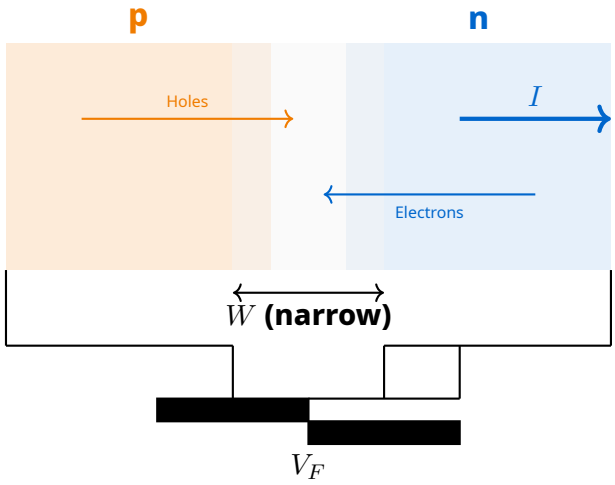


Figure 9: A p-n junction under forward bias. The battery voltage opposes the barrier potential, reducing the depletion width and causing a large current to flow.

3.4.2 Reverse Bias

In reverse bias, the p-side is connected to the negative terminal and the n-side to the positive terminal.

Reverse Biased p-n Junction

Effect:

- The applied voltage aids the internal barrier potential V_{bi}.
- The effective barrier height increases to $q(V_{bi} + V)$.
- The depletion region width **increases**.
- Majority carriers are pulled away from the junction. The diffusion current drops to nearly zero.

- A very small **reverse saturation current (I_s)** flows due to minority carriers. This current is almost constant with voltage but highly dependent on temperature.

Current:

$$I \approx -I_s \text{ (small and nearly constant)}$$

For Si, I_s is typically in nA (10^{-9} A), for Ge in μA (10^{-6} A).

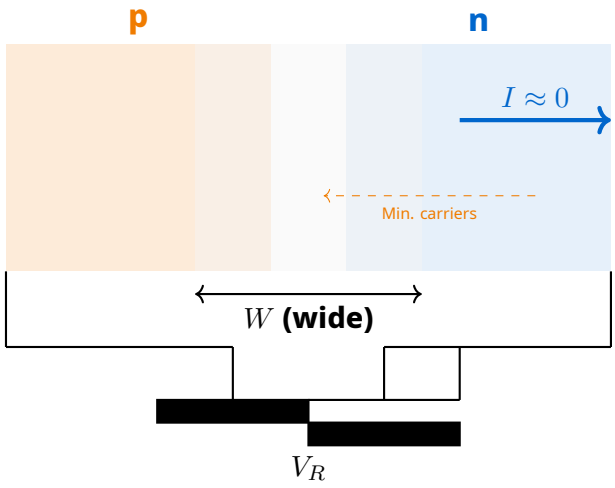


Figure 10: A p-n junction under reverse bias. The voltage increases the barrier, widening the depletion region, and only a tiny leakage current flows.

3.5 V-I Characteristics of a p-n Junction Diode

The current through an ideal p-n junction diode is described by the Shockley diode equation, which combines the forward and reverse bias behaviours.

Diode Current Equation (Shockley Equation)

$$\boxed{I = I_s \left(e^{\frac{qV}{\eta k_B T}} - 1 \right)}$$

Where:

- I_s = reverse saturation current.
- V = applied voltage (positive for forward bias).
- q = charge of an electron (1.6×10^{-19} C).
- k_B = Boltzmann's constant (1.38×10^{-23} J/K).
- T = temperature in Kelvin.
- η = ideality factor (1 for Ge, ≈ 2 for Si at low currents).

Simplified Behaviours:

- **Forward Bias ($V > 0$):** $e^{qV/\eta k_B T} \gg 1$, so $I \approx I_s e^{qV/\eta k_B T}$ (exponential rise).
- **Reverse Bias ($V < 0$):** $e^{-q|V|/\eta k_B T} \ll 1$, so $I \approx -I_s$ (constant, reverse saturation current).

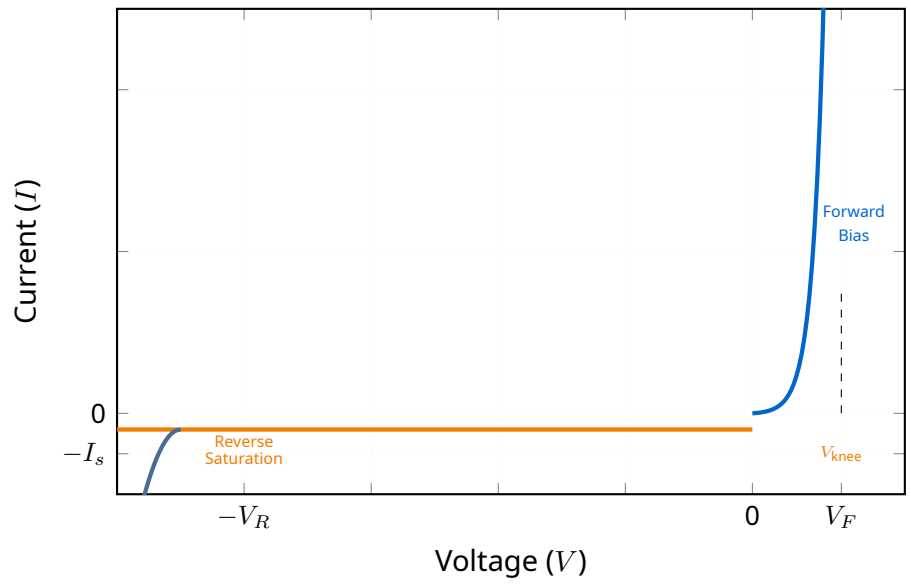


Figure 11: The V-I characteristic curve of a p-n junction diode. The graph shows the exponential forward current, the reverse saturation current, and the eventual breakdown at high reverse voltage.

Key Diode Parameters

1. **Knee Voltage / Cut-in Voltage:** The minimum forward voltage required to make the diode conduct significantly. Si: ~ 0.7 V, Ge: ~ 0.3 V.
2. **Dynamic Resistance (r_d):** The resistance offered by the diode to an AC signal.
$$r_d = \frac{\Delta V}{\Delta I}$$
3. **Breakdown Voltage:** The reverse voltage at which the current increases sharply, potentially damaging the diode (unless it's a Zener diode).

4 Special Purpose p-n Junction Diodes

Beyond the basic rectifier diode, there are several types of diodes engineered to exploit specific properties of the p-n junction. We will discuss the Zener diode, Photodiode, Light Emitting Diode (LED), and Solar Cell.

4.1 Zener Diode

A Zener diode is a specially fabricated p-n junction diode that is designed to operate reliably in the **reverse breakdown region** without getting damaged.

Zener Breakdown and Zener Diode

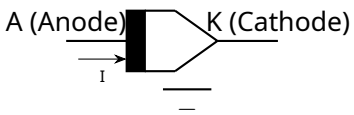
Zener Breakdown:

- In a heavily doped p-n junction, the depletion region is very thin.
- A relatively small reverse voltage (typically $< 5 - 6$ V) creates an extremely strong electric field ($\sim 10^6$ V/m) across this thin depletion region.
- This field is strong enough to directly pull (or "rip") valence electrons from their covalent bonds, creating a large number of electron-hole pairs. This sudden surge in current is called **Zener breakdown**.

Zener Diode as a Voltage Regulator:

- A Zener diode is designed to have a sharp, well-defined breakdown voltage, called the **Zener voltage (V_Z)**.
- In the breakdown region, the voltage across the Zener diode remains nearly constant (V_Z) over a wide range of reverse current.
- This property makes it an excellent **voltage regulator**, maintaining a constant output voltage despite variations in input voltage or load current.

Circuit Symbol:



4.2 Photodiode

A photodiode is a p-n junction diode operated in **reverse bias** that converts light energy into electrical energy (current).

Working Principle of a Photodiode

- A photodiode is constructed with a transparent window that allows light to fall on the junction.
- When light photons with energy $h\nu > E_g$ (the band gap) strike the depletion region, they are absorbed and create **electron-hole pairs (EHPs)**.

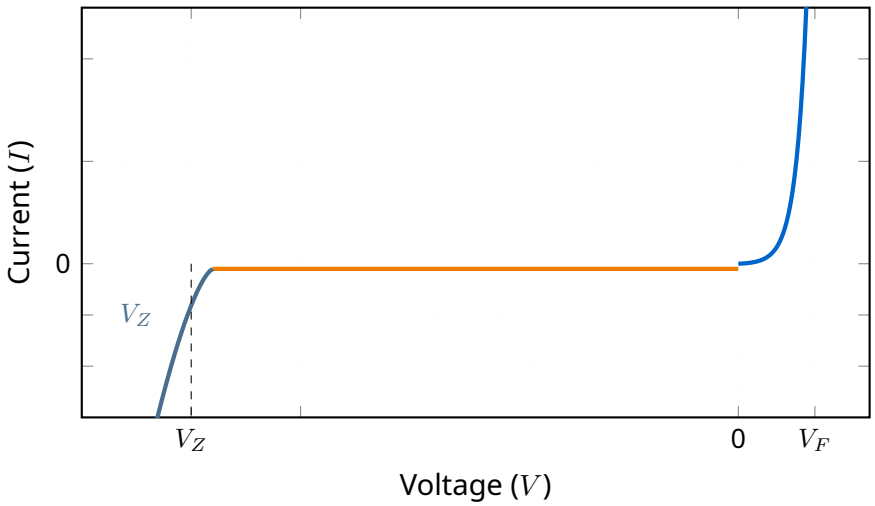
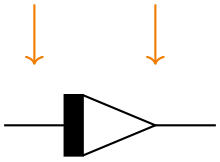


Figure 12: V-I characteristic of a Zener diode. Notice the extremely sharp breakdown at the Zener voltage (V_Z) in the reverse bias region.

- The strong electric field in the reverse-biased depletion region immediately separates these carriers—electrons move to the n-side, holes to the p-side.
- This creates an additional current flow, called the **photocurrent (I_p)**, which is directly proportional to the incident light intensity.
- The total reverse current is $I = I_s + I_p$. In the absence of light, only a tiny dark current (I_s) flows.

Circuit Symbol:



4.3 Light Emitting Diode (LED)

An LED is a heavily doped p-n junction diode operated in **forward bias** that converts electrical energy directly into light energy.

Working Principle of an LED

- When an LED is forward biased, electrons from the n-region and holes from the p-region are injected across the junction.
- These excess minority carriers recombine with the majority carriers in the depletion region and adjacent neutral regions.
- In direct band gap semiconductors (like GaAs, GaP), this recombination

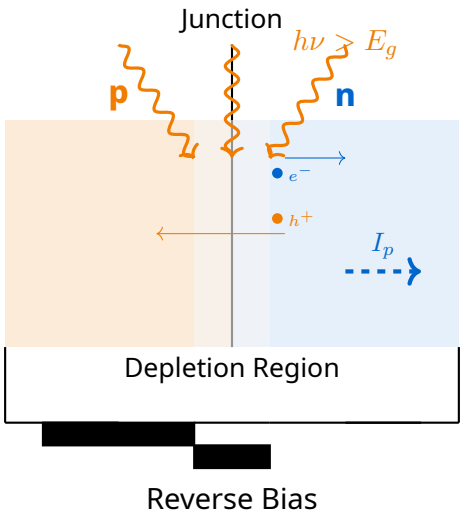


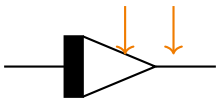
Figure 13: A reverse-biased photodiode. Photons generate electron-hole pairs in the depletion region, which are separated by the field to produce a photocurrent (I_p).

is **radiative**, meaning the energy released is emitted as a photon of light.

- The wavelength (and therefore colour) of the emitted light is determined by the energy band gap of the material used:

$$\lambda = \frac{hc}{E_g}$$

Circuit Symbol:



NCERT Nugget: LED Materials and Colours

The band gap of the semiconductor determines the colour:

Material	Band Gap E_g (eV)	Colour Emitted
GaAs (Gallium Arsenide)	1.4	Infrared (IR)
GaAsP (Gallium Arsenide Phosphide)	1.8–2.0	Red to Yellow
GaP (Gallium Phosphide)	2.26	Green
InGaN (Indium Gallium Nitride)	2.8–3.2	Blue to White

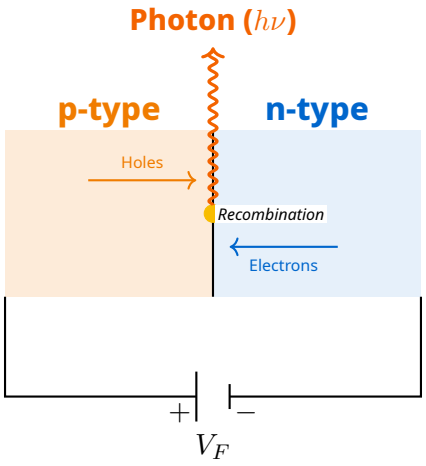


Figure 14: Working of a forward-biased LED. Recombination of electrons and holes in the junction region releases energy in the form of photons.

4.4 Solar Cell

A solar cell is essentially a large-area p-n junction diode operated with no external bias, designed to convert sunlight directly into electrical power.

Working Principle of a Solar Cell

- It works on the same principle as a photodiode (photovoltaic effect), but it is optimized for power generation.
- Light illuminates the junction, creating EHPs in the depletion region.
- The internal electric field (V_{bi}) separates the carriers, causing a **photovoltage (V_{oc})** to develop across the terminals.
- When a load is connected, the photocurrent (I_{sc}) flows through it, delivering electrical power.

Key Parameters:

- I_{sc} **(Short Circuit Current):** The maximum current when $V = 0$. Proportional to light intensity.
- V_{oc} **(Open Circuit Voltage):** The maximum voltage when $I = 0$. Typically 0.5–0.6 V for Si.
- **Fill Factor (FF):** Measures the "squareness" of the I-V curve.
- **Efficiency (η):** $\eta = \frac{P_{\text{max}}}{P_{\text{in}}} = \frac{V_{oc} I_{sc} FF}{\text{Light Intensity} \times \text{Area}}$.

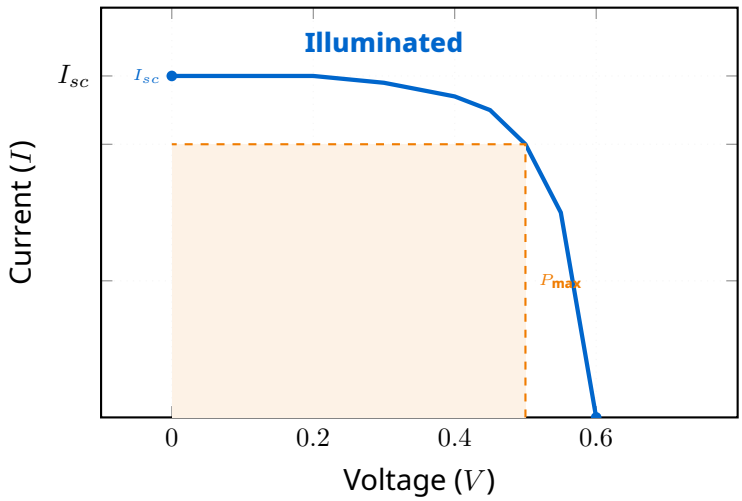


Figure 15: Current-Voltage (I-V) characteristic of a solar cell in the fourth quadrant (power generation mode). The shaded rectangle represents the maximum power point (P_{max}).

Comparison of Special Diodes

Device	Bias Condition	Primary Function	Key Application
Zener Diode	Reverse	Voltage regulation	Voltage stabilizers, surge protectors
Photodiode	Reverse	Light detection	Burglar alarms, CD players, smoke detectors
LED	Forward	Light emission	Displays, indicators, lighting
Solar Cell	Zero (unbiased)	Power generation	Solar panels, renewable energy

5 Junction Transistor

5.1 Introduction and Structure

A transistor is a three-terminal semiconductor device that can amplify an electrical signal or act as an electronic switch. It is the fundamental building block of modern electronics. The Bipolar Junction Transistor (BJT) was invented in 1947 by John Bardeen, Walter Brattain, and William Shockley at Bell Laboratories.

Bipolar Junction Transistor (BJT)

A **BJT** consists of two back-to-back p-n junctions formed by sandwiching a thin layer of one type of semiconductor between two thicker layers of the opposite type. There are two types:

1. **n-p-n Transistor:** A thin p-type region is sandwiched between two n-type regions.
2. **p-n-p Transistor:** A thin n-type region is sandwiched between two p-type regions.

The Three Regions and Terminals:

- **Emitter (E):** Heavily doped and of moderate size. It injects majority charge carriers into the base.
- **Base (B):** Very thin ($\sim 1\mu$m) and lightly doped. It controls the flow of carriers from emitter to collector.
- **Collector (C):** Moderately doped and the largest in size. It collects the majority charge carriers injected by the emitter.

Note: We will focus primarily on the n-p-n transistor, as it is more commonly used due to higher electron mobility. The working of a p-n-p transistor is analogous, with holes as the primary charge carriers and opposite voltage polarities.

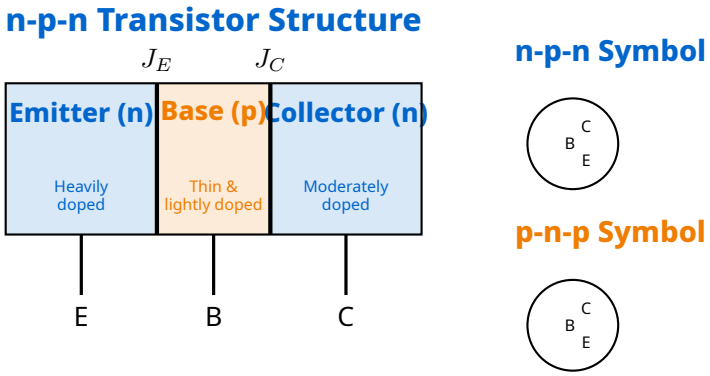


Figure 16: Physical structure and standard circuit symbols for BJT transistors. Note the arrow on the emitter indicates the direction of conventional current (P to N).

5.2 Basic Working Principle of an n-p-n Transistor

The transistor is operated by biasing the two junctions appropriately. For an n-p-n transistor in the **active region** (used for amplification):

Transistor Biasing and Current Flow

1. **Emitter-Base Junction (Forward Biased):** The n-type emitter is connected to the negative terminal of V_{EE}, and the p-type base to the positive terminal. This forward bias reduces the depletion width of J_E, causing a large number of **electrons** to be injected from the emitter into the thin base region.
2. **Base-Collector Junction (Reverse Biased):** The p-type base is connected to the negative terminal of V_{CC}, and the n-type collector to the positive terminal. This reverse bias creates a strong electric field in the depletion region of J_C.
3. **Diffusion and Collection:** The electrons injected into the base are minority carriers there. About 95% to 99% of these electrons **diffuse** through the extremely thin base, reach the collector junction, and are immediately swept across into the collector by the strong reverse bias field. This forms the **collector current (I_C)**.
4. **Base Current:** A small fraction (1% to 5%) of the injected electrons recombine with holes in the base. A small flow of positive charge enters the base terminal to replenish these holes, forming the **base current (I_B)**.

Key Transistor Equation:

$$\boxed{I_E = I_B + I_C}$$

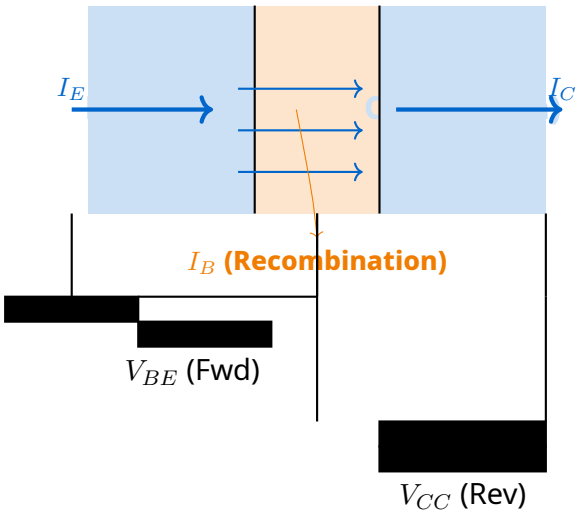


Figure 17: Current flow in a properly biased n-p-n transistor. Most electrons from the emitter traverse the thin base and are collected, making $I_C \approx I_E$.

5.3 Transistor Configurations

A transistor can be connected in three distinct ways, depending on which terminal is common to both the input and output circuits. Each configuration offers different characteristics.

Common Base (CB) Configuration

- **Input:** Between Emitter and Base (V_{EB} or V_{BE}, depending on n-p-n/p-n-p).
- **Output:** Between Collector and Base (V_{CB}).
- **Current Gain (α):** The ratio of collector current change to emitter current change at constant V_{CB}.

$$\alpha = \left(\frac{\Delta I_C}{\Delta I_E}\right)_{V_{CB}}$$

α is typically 0.95 to 0.99. It is always less than 1.

Common Emitter (CE) Configuration

- **Input:** Between Base and Emitter (V_{BE}, I_B).
- **Output:** Between Collector and Emitter (V_{CE}, I_C).
- **Current Gain (β):** The ratio of collector current change to base current change at constant V_{CE}.

$$\beta = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{V_{CE}}$$

β is typically 20 to 500. It is much greater than 1, making the CE configuration excellent for amplification.

Relation between α and β

Starting from $I_E = I_B + I_C$, we can derive:

$$\beta = \frac{\alpha}{1-\alpha}$$
$$\alpha = \frac{\beta}{1+\beta}$$

For example, if $\alpha = 0.98$, then $\beta = 0.98/(0.02) = 49$.

5.4 Transistor as an Amplifier (CE Configuration)

The CE configuration is most widely used for voltage, current, and power amplification.

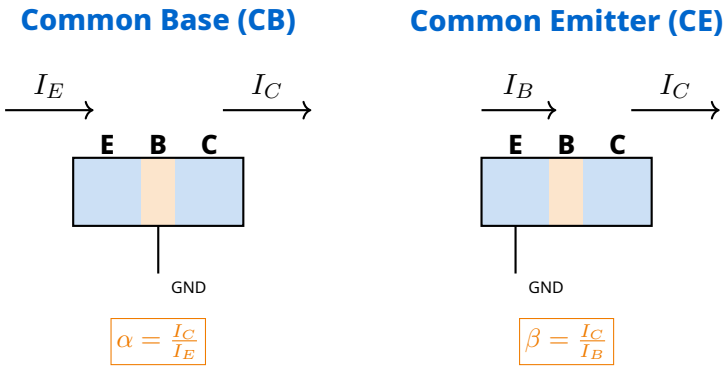


Figure 18: Simplified block diagrams for Common Base (CB) and Common Emitter (CE) configurations.

Working of a CE Amplifier

- A small, time-varying input signal voltage (v_i) is applied in series with the base-emitter forward bias (V_{BB}).
- This causes a small variation (ΔI_B) in the base current.
- Due to transistor action, this produces a large variation ($\Delta I_C = \beta \Delta I_B$) in the collector current.
- This large ΔI_C flows through a large load resistance (R_C) connected between the collector and V_{CC}.
- The output voltage ($v_o = V_{CC} - I_C R_C$) undergoes a large variation. Thus, the weak input signal is amplified.
- The phase difference between the output voltage and input voltage is 180° (π radians) in a CE amplifier.

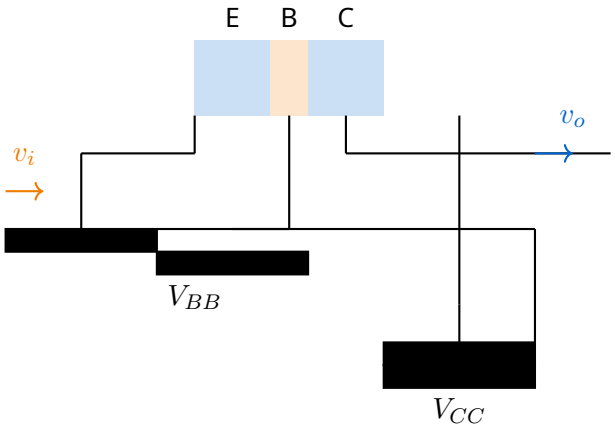


Figure 19: A simple Common Emitter (CE) amplifier circuit. A small input signal v_i at the base controls a large collector current, producing an amplified output v_o across R_C.

5.5 Transistor as a Switch

Besides amplification, a transistor in CE configuration can act as an efficient electronic switch.

Switching Operation

A transistor can be toggled between two states:

- **Cut-off State (OFF):** The input base current $I_B = 0$. Therefore, $I_C \approx 0$. The transistor acts like an open switch between collector and emitter. The output voltage $V_o = V_{CC}$ (HIGH).
- **Saturation State (ON):** The input voltage is high enough to drive a large base current. I_C reaches its maximum value $I_{C(\text{sat})} = V_{CC}/R_C$. The transistor acts like a closed switch. The collector-emitter voltage $V_{CE} \approx 0$ (LOW).

This binary OFF/ON behaviour is the basis for digital logic circuits (0 and 1 states).

Key Transistor Parameters to Remember

Parameter	Symbol	Definition	Formula
Input Resistance	R_i	$\Delta V_{BE}/\Delta I_B$	Low in CE ($\sim k\Omega$)
Output Resistance	R_o	$\Delta V_{CE}/\Delta I_C$	High in CE ($\sim 10 - 100\ k\Omega$)
Current Gain (CB)	α	$\Delta I_C/\Delta I_E$	$< 1, \approx 0.98$
Current Gain (CE)	β	$\Delta I_C/\Delta I_B$	$\gg 1, \approx 100$
Voltage Gain (CE)	A_v	$\Delta V_{CE}/\Delta V_{BE}$	$-\beta\frac{R_C}{R_i}$

6 Digital Electronics and Logic Gates

6.1 Analog vs. Digital Signals

Electronic signals can be broadly classified into two categories, which determines how information is processed in a circuit.

Analog and Digital Signals

1. **Analog Signal:** A continuous signal whose amplitude varies smoothly with time. At any instant, it can have any value within a given range.
   - Example: The output voltage from a microphone, a sine wave.
2. **Digital Signal:** A discontinuous signal that has only two discrete levels—a HIGH state and a LOW state.
   - Typically represented as bits: HIGH = 1 (e.g., $+5$ V) and LOW = 0 (e.g., 0 V).
   - This binary nature makes it robust against noise and forms the language of computers and digital systems.

Logic Gate: A digital circuit that performs a specific logical operation on one or more binary inputs to produce a single binary output. Logic gates are the fundamental building blocks of digital electronics.

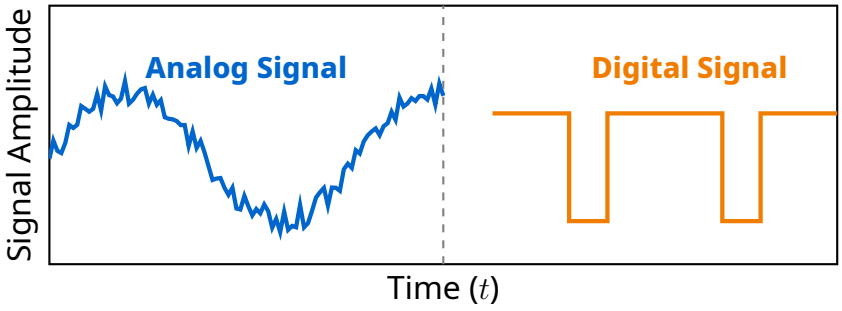


Figure 20: Comparison of an analog signal (smooth, continuous) and a digital signal (discrete, two-level square wave).

6.2 Boolean Algebra and Basic Logic Operations

Boolean algebra, developed by George Boole, is the mathematical framework for describing the behaviour of logic circuits. It deals with binary variables (0 and 1) and three fundamental operations.

The Three Fundamental Logic Gates

1. **NOT Gate (Inverter):** The output is the complement (inverse) of the input.
$$Y = \bar{A}$$
2. **AND Gate:** The output is HIGH (1) only when **all** inputs are HIGH (1).
$$Y = A \cdot B$$
3. **OR Gate:** The output is HIGH (1) when **any one or more** of the inputs

are HIGH (1).

$$Y = A + B$$

From these, two universal gates can be derived by the principle of negation:

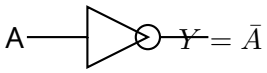
1. **NAND Gate:** AND followed by NOT.
2. **NOR Gate:** OR followed by NOT.
3. **XOR and XNOR Gates:** For exclusive OR and exclusive NOR operations.

6.3 Detailed Study of Logic Gates

Let's examine the symbol, truth table, and practical electronic realization (using diodes and transistors) for each primary gate.

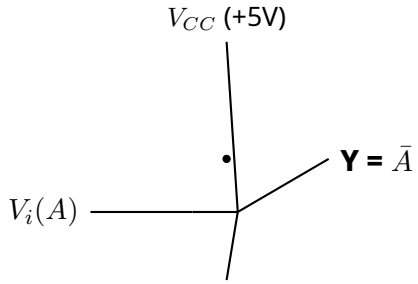
6.3.1 NOT Gate

NOT Gate (Inverter)



Operation: The output is the logical inverse of the input. If $A = 0$, $Y = 1$; if $A = 1$, $Y = 0$.
Transistor Circuit: A simple CE transistor can act as a NOT gate. When the input at the base is HIGH ($V_i = 5$V), the transistor saturates, pulling the output LOW ($V_o \approx 0$). When input is LOW, the transistor is cut-off and the output is pulled HIGH by R_C.

NOT Gate (Transistor Inverter)



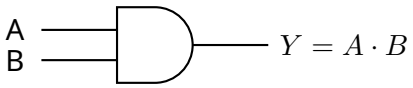
Truth Table

A	Y
0	1
1	0

Figure 21: A transistor-based NOT gate circuit and its corresponding truth table.

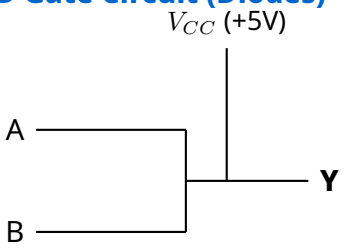
6.3.2 AND Gate

AND Gate



Operation: Output is 1 only if both A AND B are 1.
Diode Circuit: Two diodes connected to a common resistor. If either A or B is LOW (0V), the corresponding diode conducts, pulling the output LOW. Only if both A and B are HIGH (so both diodes are reverse biased), the output is pulled HIGH by the resistor.

AND Gate Circuit (Diodes)



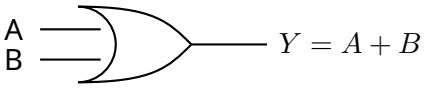
Truth Table

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

Figure 22: Refined diode-based AND gate circuit with separated labeling and truth table.

6.3.3 OR Gate

OR Gate

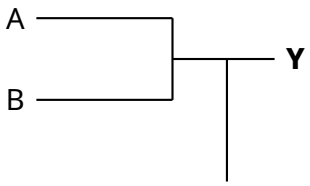


Operation: Output is 1 if either A OR B (or both) is 1.
Diode Circuit: Two diodes connected in parallel to a common resistor, but with opposite polarity to the AND gate. If either input A or B is HIGH, the corresponding diode conducts, pulling the output HIGH. Only if both are LOW, the output stays LOW.

6.3.4 NAND and NOR Gates (Universal Gates)

NAND and NOR gates are called **universal gates** because any other logic gate (AND, OR, NOT, XOR) can be implemented using only NAND gates or only NOR gates.

OR Gate Circuit (Diodes)



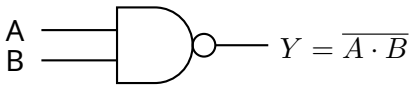
Truth Table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

Figure 23: A diode-based OR gate circuit and its logic truth table.

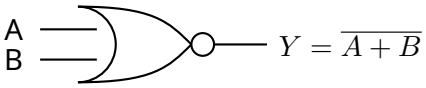
NAND and NOR Gates

NAND Gate:



$$Y = \overline{A \cdot B}$$

NOR Gate:



$$Y = \overline{A + B}$$

NAND Gate Truth Table

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

NOR Gate Truth Table

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Figure 24: Truth tables for the NAND and NOR gates.

6.4 Summary of Logic Gates

It is essential to have a quick comparative reference for all seven basic logic gates.

Complete Logic Gate Summary (2-Input)

Gate	Symbol	Boolean	Output Y = 1 when...	Output Y = 0 when...
NOT		$Y = \bar{A}$	A = 0	A = 1
AND		$Y = A \cdot B$	A=1 AND B=1	Any input is 0
OR		$Y = A + B$	A=1 OR B=1	A=0 AND B=0
NAND		$Y = \overline{AB}$	Any input is 0	A=1 AND B=1
NOR		$Y = \overline{A + B}$	A=0 AND B=0	Any input is 1
XOR		$Y = A \oplus B$	Inputs differ	Inputs same
XNOR		$Y = \overline{A \oplus B}$	Inputs same	Inputs differ

7 Integrated Circuits

7.1 What is an Integrated Circuit?

The invention of the transistor miniaturized electronics, but circuits still required many discrete components (transistors, diodes, resistors, capacitors) connected by wires on a circuit board. The next revolutionary step was to fabricate an entire circuit on a single piece of semiconductor material.

Integrated Circuit (IC)

An **Integrated Circuit (IC)** is a miniature, complete electronic circuit consisting of active components (like transistors and diodes) and passive components (like resistors and capacitors), all fabricated on a single tiny semiconductor chip (typically silicon) and interconnected to perform a specific function.

- The chip is hermetically sealed in a protective package, from which external connecting pins emerge.
- This technology is often called a **monolithic IC** (mono = single, lithos = stone).
- ICs can be classified based on their function as **Analog (Linear) ICs**

(e.g., operational amplifiers, voltage regulators) or **Digital ICs** (e.g., microprocessors, memory chips).

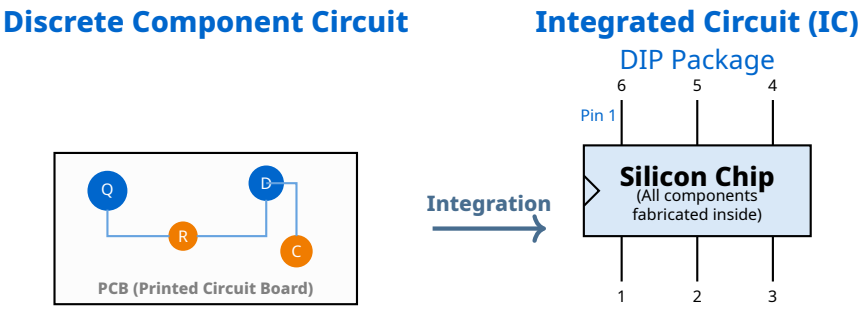


Figure 25: Comparison between discrete components on a PCB and an integrated circuit (IC) where all components are scaled down and fabricated onto a single silicon substrate.

7.2 Scale of Integration

The complexity and power of ICs have grown exponentially since their invention, following Moore's Law (proposed by Gordon Moore in 1965). This is classified based on the number of logic gates or transistors packed into a single chip.

Evolution and Classification of ICs

1. **SSI (Small Scale Integration):** Early ICs containing a few logic gates (fewer than 10 gates or about 10-100 transistors). Examples: Basic logic gates like 7400 (NAND), 7408 (AND).
2. **MSI (Medium Scale Integration):** Contains 10 to 100 gates (100 to 1000 transistors). Examples: Adders, multiplexers, decoders, counters.
3. **LSI (Large Scale Integration):** Contains 100 to 1000 gates (1,000 to 10,000 transistors). Examples: Early 8-bit microprocessors (Intel 8085), small memory chips.
4. **VLSI (Very Large Scale Integration):** Contains 1,000 to over a million gates (10,000 to billions of transistors). Examples: Modern microprocessors (Intel Core i7, Apple M-series), DSP chips.
5. **ULSI (Ultra Large Scale Integration):** Contains over a million gates (billions of transistors). This term is often used interchangeably with advanced VLSI.

7.3 Advantages of Integrated Circuits

The shift from discrete electronic components to ICs revolutionized electronics. The advantages are profound.

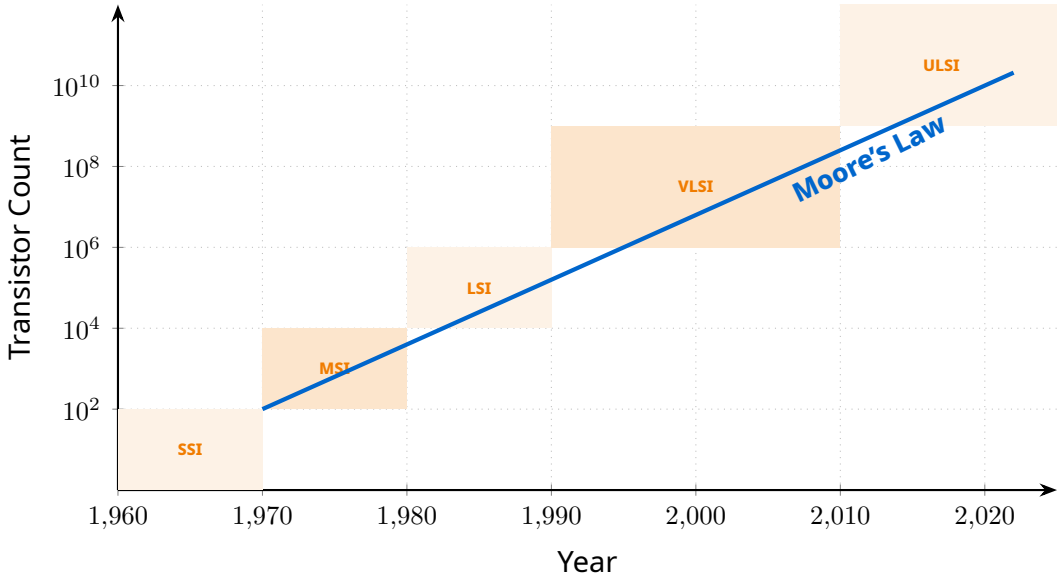


Figure 26: Moore's Law trend showing the evolution from Small Scale Integration (SSI) to Ultra Large Scale Integration (ULSI).

Why ICs Replaced Discrete Circuits

1. **Miniaturisation:** Extremely small size and weight. A circuit that once occupied a large board can fit in a few square millimeters.
2. **Cost:** Mass production using photolithography makes complex circuits incredibly cheap per function.
3. **Reliability:** Billions of components are fabricated simultaneously, eliminating soldered joints which are a primary source of failure. ICs have a very long operational life.
4. **Speed & Performance:** The components are extremely close, minimizing parasitic capacitance and signal propagation delay, leading to high operating speeds.
5. **Power Consumption:** Very low power is required due to the small size and optimized circuits.
6. **Ease of Replacement:** It is often simpler and more cost-effective to replace a faulty IC than to troubleshoot and repair a complex discrete circuit.

7.4 Limitations and the Future

While ICs have transformed technology, they do have limitations that drive ongoing research.

Limitations of ICs

1. **Power Dissipation:** Dissipating heat from billions of densely packed transistors is a major challenge, limiting clock speeds (the "power wall").
2. **Fabrication of Passive Components:** It's difficult to fabricate inductors or large-value capacitors on a chip. These are often external components.
3. **Quantum Limits:** As transistor sizes shrink towards atomic scales (gate lengths of a few nanometers), quantum mechanical effects like electron tunneling cause undesirable leakage currents, challenging the fundamental operation of the transistor.
4. **Flexibility:** Once fabricated, an IC cannot be modified or easily reconfigured, unlike a circuit made of discrete components.

Key Fact: The Silicon Wafer

The foundation of every IC is an ultra-pure, defect-free single crystal of silicon, grown in a cylindrical shape (an ingot) and then sliced into thin, mirror-polished **wafers**. Typical wafer diameters are 150 mm, 200 mm, and 300 mm. Hundreds or thousands of identical ICs are fabricated simultaneously on a single wafer through a complex sequence of photolithography, etching, doping, and metal deposition.

8 NCERT Solved Examples

Example 14.1: Intrinsic Carrier Concentration in Si

Problem: Pure silicon at 300 K has equal electron (n_i) and hole (p_i) concentrations of 1.5×10^{16} m^{-3}. Doping by indium increases p_h to 4.5×10^{22} m^{-3}. Calculate n_e in the doped silicon.
Solution:

$$\text{Mass-action law: } n_e p_h = n_i^2$$

$$n_e = \frac{n_i^2}{p_h}$$

$$= \frac{(1.5 \times 10^{16})^2}{4.5 \times 10^{22}}$$

$$= \frac{2.25 \times 10^{32}}{4.5 \times 10^{22}} = 5.0 \times 10^{9} \text{ m}^{-3}$$

The electron concentration drops dramatically in the doped p-type semiconductor.

Example 14.2: p-n Junction Forward Bias Current

Problem: The V-I characteristic of a silicon diode is given in the figure. Calculate the resistance of the diode at (a) $I_D = 15$ mA and (b) $V_D = -10$ V.
Solution:

(a) From the curve (forward bias), at $I = 15$ mA, $V \approx 0.7$ V.

$$r_f = \frac{V}{I} = \frac{0.7\ \text{V}}{15 \times 10^{-3}\ \text{A}} \approx 46.7\,\Omega$$

(b) At $V = -10$ V, the reverse saturation current is almost constant at $I_s \approx -1\,\mu$A.

$$r_r = \frac{10\ \text{V}}{1 \times 10^{-6}\ \text{A}} = 10\,\text{M}\Omega$$

Conclusion: The diode has a very low resistance in forward bias and a very high resistance in reverse bias, acting as a one-way switch.

Example 14.3: Zener Diode as a Voltage Regulator

Problem: A 6 V Zener diode is used in the voltage regulator circuit shown. The input voltage varies from 10 V to 16 V, and the load current varies from 4 mA to 20 mA. Calculate the series resistance R_s required for proper regulation. Assume $I_{Z(\text{min})} = 2$ mA. (A circuit is assumed).
Solution:

Total current through R_s : $I_{\text{total}} = I_L + I_Z$

Maximum I_{total} : $I_{\text{max}} = I_{L(\text{max})} + I_{Z(\text{min})} = 20 + 2 = 22$ mA

The maximum current occurs at minimum input voltage to ensure the Zener just stays in breakdown.

$$R_s = \frac{V_{i(\text{min})} - V_Z}{I_{\text{max}}}$$
$$= \frac{10\ \text{V} - 6\ \text{V}}{22 \times 10^{-3}\ \text{A}} = \frac{4}{0.022} \approx 182\,\Omega$$

A standard resistor value of $180\,\Omega$ can be used.

Chapter 14: Key Concepts to Master

1. **Energy Bands:** The conduction difference between conductors, semiconductors ($E_g \approx 1$ eV), and insulators ($E_g > 3$ eV).
2. **Doping:** n-type (pentavalent, e.g., P) gives extra electrons. p-type (trivalent, e.g., B) creates holes.
3. **p-n Junction:** The formation of the depletion region, barrier potential (V_{bi}), and the behaviour under forward and reverse bias.

4. **Rectifier:** A p-n junction diode acts as a rectifier, converting AC to DC.
5. **Zener Diode:** Heavily doped, operates in breakdown region for voltage regulation.
6. **Optoelectronic Devices:** LEDs (forward bias, electrical to light) and Photodiodes (reverse bias, light to electrical current).
7. **Transistor:** The three-terminal device (Emitter, Base, Collector). The relation $I_E = I_B + I_C$ and current gain $\beta = I_C/I_B$.
8. **Logic Gates:** The building blocks of digital electronics—NOT, AND, OR, NAND, NOR.
9. **ICs:** The integration of millions of components on a single chip, driving the digital revolution.